

PowerPro: RTL全ての段階でローパワー化の支援と管理

フィジカルを考慮したパワー解析

RTL論理設計

ゲート

レイアウト

マニュアル・パワー最適化を支援

自動最適化

```

1 module adder
2   #(length = 4)
3   (input wire [length-1:0] a, b,
4    output logic [length-1:0] sum,
5    output logic overflow);
6
7   logic [length-1:-1] carry;
8
9   always @(a or b)
10    begin
11      carry[-1] = 0;
12      for (int i=0; i<length; i = i+1)
13        begin :addloop
14          sum[i] = a[i] ^ b[i] ^ carry[i-1];
15          carry[i] = ((a[i]^b[i]) & carry[i-1]) | (a[i] & b[i]));
16        end : addloop
17      overflow = carry[length-1] ^ carry[length-2];
18    end
19 endmodule :adder
    
```

パワー浪費を構造的に解析
(Power Lint)

Design Statistics		Design Power	
Number of Flops	88217	Peak Power	Not asked
User Enabled Flops	59605 (67.57 %)	Total Leakage Power	47.29 uW
Clock Gating Efficiency	70.43 %	Total Internal Power	29913.30 uW
Number of Memories	14	Total Design Power	29960.60 uW
Memory Efficiency	10.57 %		

Micro-Architectural Redundancy		Combinational Redundancy	
Block Level Clock Gating	0 uW 0 Blocks	Redundant Mux Toggles	4488 uW 249 Mux Inputs
Shift Register To Circular Buffer	2048.86 uW 2800 Flops	High Toggling Signals	1488 uW 10050 Bits
Access Profile	0 uW 0 (0%) Memories	Redundant Memory Address Toggles	0 uW 0 Inputs
Bypass Potential	0 uW 0 (0%) Memories	Redundant Memory Data Toggles	0 uW 0 Inputs

Sequential Redundancy		Metrics Driven Power Regression	
Redundant Reset	17.26 uW 5455 Flops		
Clock Gating	5582.1 uW 9803 Flops		
Data Gating	3.97 uW 6 Operators		
Stable Access	0 uW 0 Memory Enables		
Light Sleep Potential	0 uW 0 (0%) Memories		

パワー浪費を機能(動作)的に解析

- レジスタ
- メモリ

自動パワー最適化

等価性検証

ローパワーRTL

パワー・リグレッション機能