PRODUCT BROCHURE

Solving Your On-Chip Processing Challenges

At Codasip®, we live for solving your on-chip processing challenges. Our offering includes the all-purpose **Codasip Studio™** processor design environment, the family of **Codasip RISC-V Processors**, and the **SweRV Core™ Support Package** for supporting open source RISC-V cores designed by Western Digital®.

We build our solutions on open standards such as **RISC-V®** to support innovation and provide longevity. RISC-V is an open instruction set architecture (ISA) that enables you to take advantage of a standard base ISA for software portability, yet to enhance computational performance with custom extensions. As processor design experts, however, we appreciate that a different architecture may work well in your unique case, and Codasip Studio can be applied to create an optimal processor for you needs.

Today, you can no longer rely on Moore's Law to improve the performance of integrated circuits, because we are reaching the physical limits of miniaturization. Instead, you will need to innovate in domain-specific architecture in order to improve your performance and efficiency. At Codasip we provide a wide range of innovative processing solutions which can be tuned to meet your needs.

Our Portfolio

Codasip's proven solutions are powering SoCs from around the world. Find out how you too can benefit from our unique methodology!

Codasip Studio pg. 6

This tool provides a complete, highly automated tool for design and customization of processor cores.

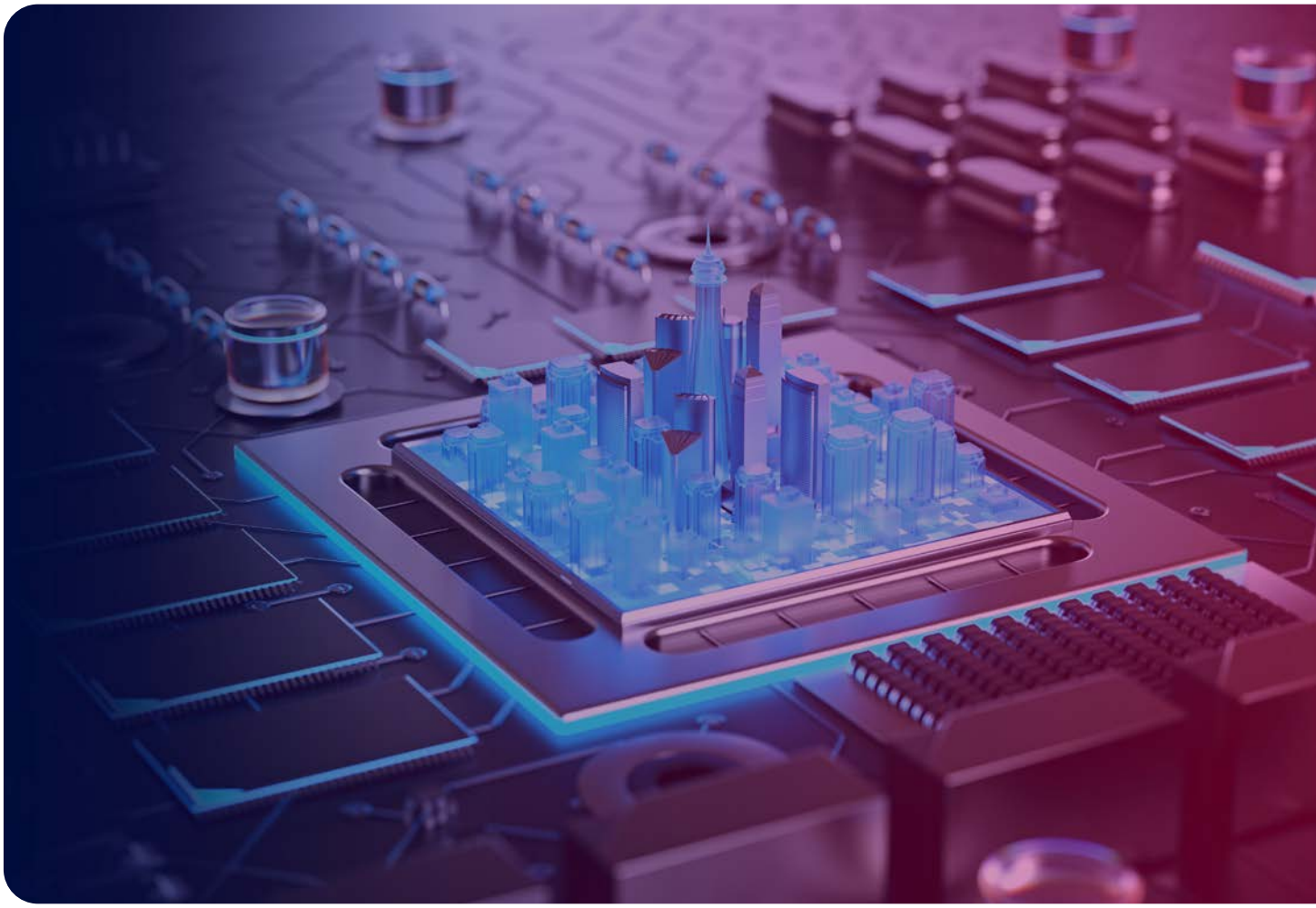
Codasip RISC-V Processors pg. 12

Our own series of ready-made designs can be deployed in standard configurations or extended and configured in Codasip Studio for a tailored result.

Codasip SweRV Core Support Package pg. 16

SweRV cores, the open RISC-V designs by Western Digital, can be deployed in a fast and risk-free fashion using our exclusive support package.

RISC-V



RISC-V
A modern Instruction Set Architecture (ISA) that is universal, flexible, and open to creating unique microarchitectures.
More information at www.riscv.org

The New Open Standard

The cornerstone of our processor family is RISC-V (pronounced risk-five). It is an open, royalty-free instruction set architecture (ISA) which offers key advantages including:

Vendor Independence & Longevity

Many ISAs are proprietary and controlled by a single vendor. This means that you are dependent on the terms as well as the health of that vendor and you face a closed ecosystem. The RISC-V ISA is vendor- independent, giving you freedom of choice and no dependency on the survival of a single company.

This also means that any software you target to the base instruction set or to standard extensions is guaranteed to run on all current and future Codasip processor cores, eliminating hidden redesign costs and ISA incompatibilities. The RISC-V ecosystem has enjoyed support from many strong industry players, bringing maturity and true longevity.

Modularity & Extensibility

The RISC-V ISA includes base instructions that are always present in addition to a number of standard extensions such as multiplication & division [M], atomic instructions [A], compressed [C], single-precision floating point [F] and double-precision floating point [D].

This modularity enables you to decide which extensions add value for your application and to adjust your processor design accordingly.

The RISC-V ISA additionally allows you to create custom instructions enabling you to achieve your performance, power, or area goals.

Custom Microarchitecture

Since the RISC-V ISA does not specify a microarchitecture, you can choose variations such as pipeline depth, number of threads and number of issues, caches, interrupts, power saving modes and bus interfaces in order to match the processor to your requirement.

Endless Possibilities

RISC-V's characteristics enable you to innovate freely without going down the path of an instruction set started from scratch, which would lack any existing ecosystem and support. It provides all the basic instructions that you need, leaving you to focus on creating novel instructions that help differentiate your design.

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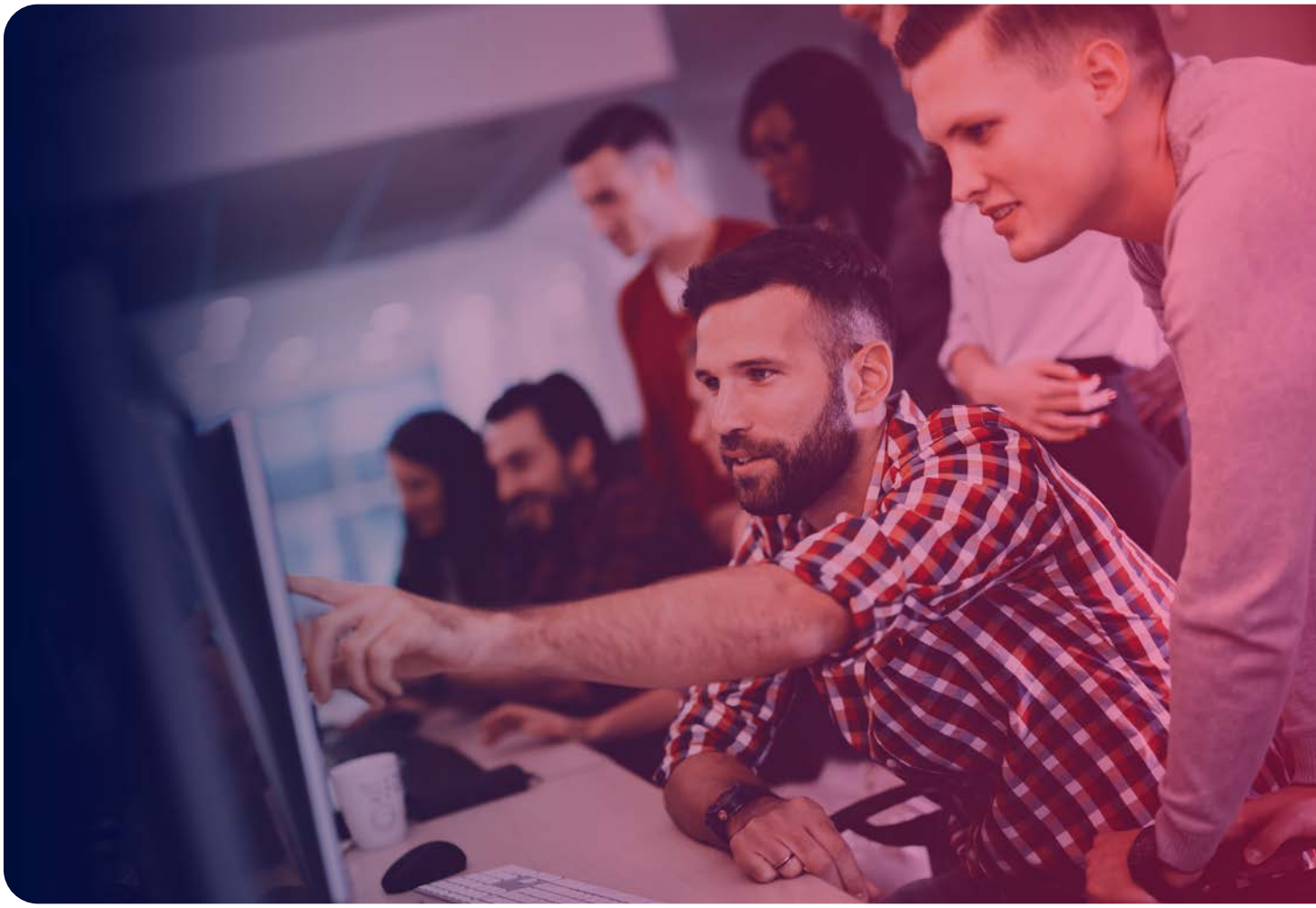
STUDIO



Codasip Studio
A complete set of Electronic Design Automation (EDA) tools for processor design automation and customization. The level of automation is unmatched on the market and the resultant RTL code is clean and human-readable.

CodAL
A C-based language for a complete processor architecture description, developed by Codasip.

Our Technology Foundation

Codasip Studio is a complete, highly automatized toolset for designing and customizing processor cores. Whether you need to create a new core or optimize an existing one, Codasip Studio makes the task unbeatably fast and easy, with reliable results.

Codasip Studio employs a revolutionary approach: One single high-level description of the processor replaces multiple manual tasks of writing the RTL, adding any custom instructions, updating the compiler, etc. Unlike similar tools, Codasip Studio generates the design implementation, verification environment, virtual system prototype, and a complete software toolchain fully automatically. The design methodology is protected by patents and we use it ourselves to create the Codasip processor IP.

In addition to its design capabilities, Codasip Studio includes powerful multiprocessor programming, debugging, and profiling features, enabling the most complex processors to be designed with ease.

We have built Codasip Studio upon open standards and software including Eclipse, LLVM, Verilog, SystemVerilog, and UVM.

Unmatched Automation and Efficiency

The high degree of automation makes it easy to take advantage of the power of processor design techniques. Tasks that traditionally take days or weeks, tying up specialized and expensive resources, are highly automated which significantly reduces both design time and cost. Compared to traditional manual design, Codasip Studio is an order of magnitude more effective, as shown in the customer example below.

Man-days to complete task

Deliverables	Codasip Studio Custom ISA	Manual Design Custom ISA
Architectural Exploration/Modeling	40–60	40–60
Toolchain/SDK Creation	<	80
Virtual Platform		80
Hardware Implementation (RTL)		100
UVM Environment		30
Verification	40–60	100–150
Total Man-Days	80–120	930–1010

Automatically Generated HDK & SDK

Hardware Development Kit (HDK)

- RTL (Verilog/VHDL/SystemVerilog)
- SystemVerilog UVM test environment
- Integration test bench
- Sample EDA scripts
- SystemC co-simulation model

Software Development Kit (SDK)

- C/C++ LLVM compiler (improved by Codasip)
- C/C++ Libraries (newlib)
- Assembler, disassembler, linker
- High-performance instruction set and cycle accurate simulators
- Debugger and profiler
- Documentation and ISA visualization
- Random programs used during verification

Because of the automation, Codasip Studio can be also conveniently used to maintain the SDK for legacy proprietary processors, saving considerable effort on the task.

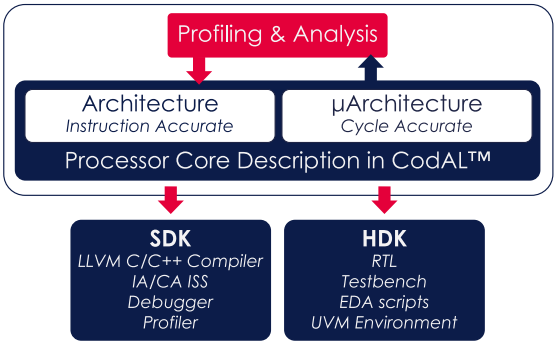
Straightforward Development Process

A unique aspect of our approach at Codasip is to automate the development of processor cores by using a high-level description language called CodAL™. The capabilities of your processor only need to be described once in CodAL, and from this single description everything needed to design, integrate, and program the processor is automatically derived. This eliminates the need for you to express the same functionality in multiple task-dependent formats and reduces traditional time-consuming manual tasks.

CodAL is a highly structured, hierarchical, C like language for processor architecture description and design. The language can describe a wide range of processor styles including **RISC, CISC, VLIW** and **DSP**.

In addition to processor descriptions, CodAL supports co-simulation with existing models as well as native modelling of multiprocessor subsystems including multiple cores, interconnect, and memory structures.

Codasip Studio Flow



A Fast Way to Outstanding Results

The key to the effectiveness of our Codasip Studio solution is the natural iterative approach to your design. Codasip Studio gives you a fast and simple way to move from your algorithm to a complete implementation. As you progress, the necessary models and tools are automatically created. Unlike alternative solutions, the generated **RTL is human-readable**.

Codasip Studio's powerful high-level processor synthesis technology allows you to generate processors that meet and even exceed the performance of hand-optimized designs. Additionally, the ability to add application-specific instructions natively into the processor pipeline delivers performance well above coprocessors, custom accelerators and traditional extensible processor approaches. Codasip's simple-to-use, yet **advanced profiling** analyses your applications to determine potential optimizations to either the applications or the processor implementation.

Complete Software Infrastructure

Once your instruction-accurate model of the processor is available, which typically takes only days, Codasip Studio will generate a complete SDK customized for the processor. This kit can be freely used by your embedded software development teams, allowing development, debug, and execution on the target platform well ahead of silicon availability. Generated tools are latency- aware for both instruction and data access. This is critical for maximum performance on VLIW architectures where multiple instructions are executed in parallel.

Meticulous Verification

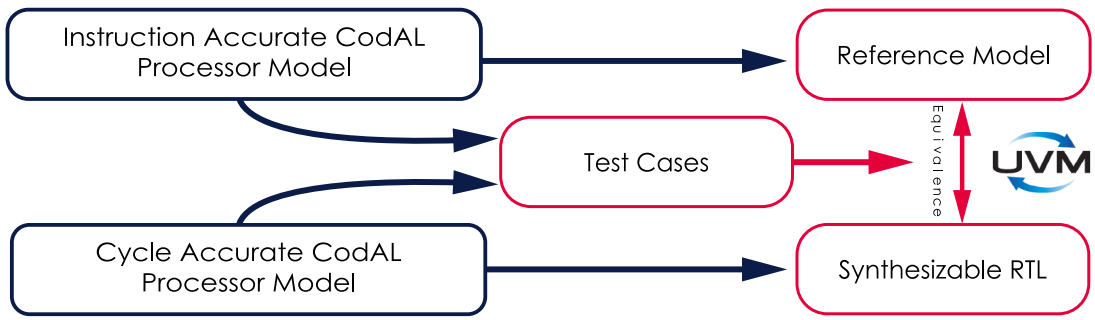
When choosing a processor (or processors) for your IC design, you will want to be assured that it has been adequately verified, for example, code and functional coverage need to be very high.

If you develop your own core using Codasip Studio or use one of our RISC-V cores developed in or modified by Studio, the quality of your core is assured by Codasip Studio's strong verification methodology. This combines a standardized approach, simulation and static checking.

Codasip Studio provides a consistency checker, random assembler program generation and an automatically generated UVM environment. UVM allows the generated RTL for your processor to be checked against your instruction-accurate reference model.

Multiple model formats are available to ensure that at each step of the verification, you have the best trade-off between viability and performance. From virtual prototyping to detailed system debug, Codasip Studio generates the models you need.

Codasip Verification Flow



Getting Beyond Moore's Law

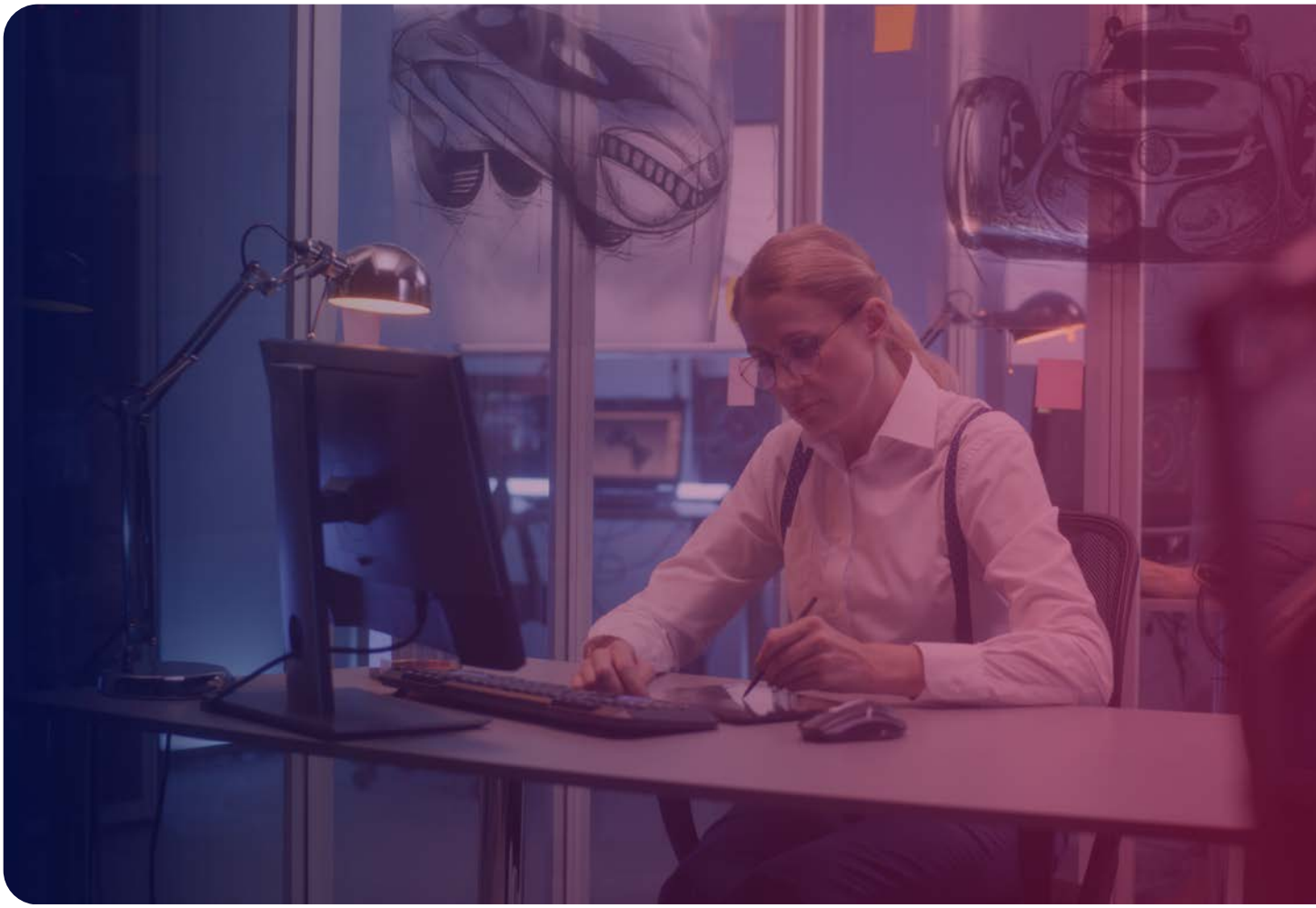
For five decades Moore's Law has predicted that the density of integrated circuits would double roughly every two years by manufacturing in smaller and smaller silicon geometries. In the past we have seen that general-purpose processors, such as the x86 or Arm architectures, have been able to handle greater and greater computational performance without a major impact to silicon costs or power consumption simply by using the latest silicon geometries.

However, in the last 5–8 years that rate of change has slowed, and Moore's Law is predicted to saturate. We now see that improving computational performance cannot simply be met by general-purpose processors in ever smaller silicon geometries. Instead, we need to be able to create custom processor architectures which are optimized to the needs of your application. You can then tune the trade-off between performance, power, and area.

Unless you are already an experienced processor designer, creating a custom ISA from scratch will be very challenging. You also face the cost of porting existing software to your new architecture. RISC-V with custom extensions offers you a development approach with both much lower risk and cost.

There is a good range of software available for the RISC-V base instruction set and you can significantly improve the performance of your application software by creating special instructions. Candidates for such special instructions include operations for cryptography, DSP, or machine learning among others. These applications are not well supported on a general-purpose processor.

PROCESSORS



Understanding Codasip's Core Portfolio

If you are looking for an off-the-shelf RISC-V core, we offer a range of different microarchitectural implementations of the RISC-V standard for virtually any requirements. Our portfolio includes two distinctive lines: the **Codasip** processor IP, and the open-source **SweRV** cores enhanced with our exclusive Support Package.

Codasip Processor Lines

	Codasip Cores	SweRV Cores
RTL	Commercially licensed	Open source
Developed by	Codasip	Western Digital
Software ecosystem	Codasip CodeSpace™	SweRV Core Support Package
Customization	Codasip Studio or on-request service	On-request service

The following table shows the complete portfolio of currently available cores, including SweRV.

Codasip Processor Portfolio at a Glance

All Cores
• Standard RISC-V debug
• JTAG (4pin/2pin)
• Compressed instructions
• AMBA buses
	Low Power Embedded
	• 32-bit
	• Up to 128 interrupts
		High Performance Embedded
		• 64-bit
		• 32-bit with performance-boosting features
		• Up to 256 interrupts
			Application
			• 64-bit
			• Floating point unit
			• Linux support:
			  • RV64GC ISA
			  • Atomic instructions
			  • Memory management unit
			  • Supervisor privilege mode

7 Series • 7–9-stage pipeline • IMC instruction set • 32 registers • Branch predictor • Parallel multiplier		SweRV Core **EH1** SweRV Core **EH2**	Codasip **A70X**™ Codasip **A70X-MP**™ Codasip **A70XP**™ Codasip **A70XP-MP**™
5 Series • 5-stage pipeline • IMC instruction set • 32 registers • Branch predictor • Parallel multiplier	Codasip **L50**™ Codasip **L50F**™	Codasip **H50X**™ Codasip **H50XF**™	
3 Series • 3–4-stage pipeline • IMC instruction set • 32 registers • Parallel multiplier	Codasip **L30**™ Codasip **L30F**™	SweRV Core **EL2**	
1 Series • 3-stage pipeline • EMC instruction set • 16 registers • Sequential multiplier	Codasip **L10**™		

Note: **X** = 64-bit, **F** = Floating Point Unit, **P** = RISC-V P Packed SIMD Extension, **MP** = Multiprocessing

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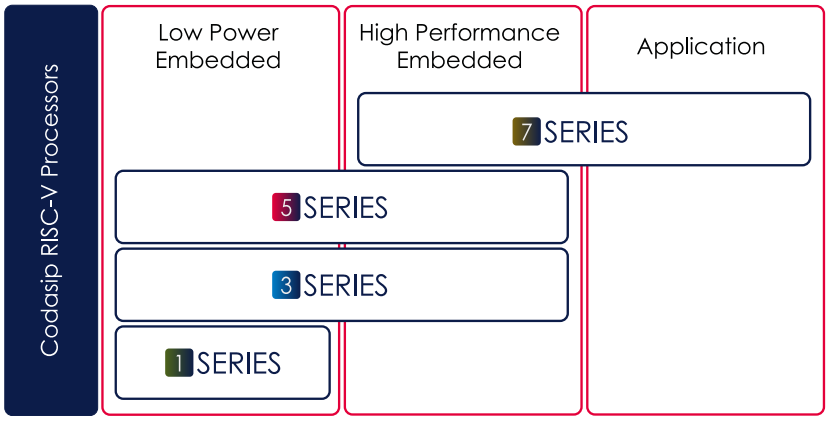
RISC-V PROCESSORS

Our Extensible Core Family

In the embedded domain, we provide cores with focus on two different primary needs: The Low Power Embedded (L) processors that are small and energy-efficient, and the High Performance Embedded (H) processors focused on performance. In addition to these, we have the advanced Application (A) cores able to run Linux.

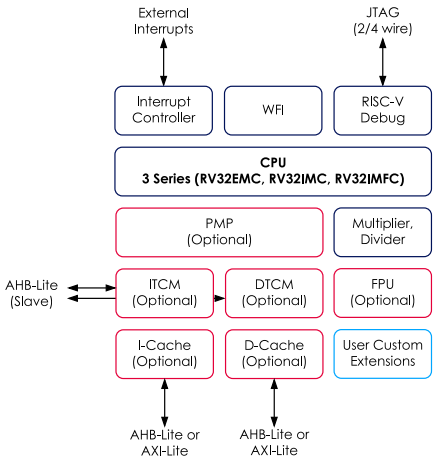
Each of the domains includes multiple series, 1 to 7, based on microarchitecture complexity. All the processors can be provided as either a fully developed and RTL-based hardware package, or as a CodAL model within the Codasip Studio environment, offering the opportunity to customize and to create your own domain-specific processor.

Codasip RISC-V Processors portfolio



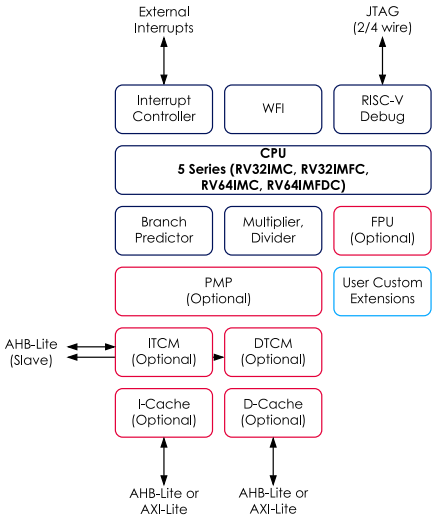
Codasip Low Power Embedded Processors

The embedded low-power domain aims to deliver minimalist, power-efficient 32-bit cores with basic integer computational capabilities and simple 3 or 5 stage pipelines. These cores support the most commonly-used RISC-V standard extensions (I/E, M & C), making them an attractive alternative to legacy, proprietary microcontroller cores.



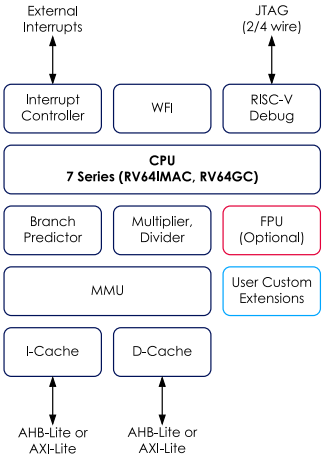
Codasip High Performance Embedded Processors

The embedded high-performance domain includes 64-bit processors as well as 32-bit processors with significantly increased integer computational performance, for example by adding the P extension. These cores feature a more complex pipeline with optional caches and dynamic branch prediction, allowing them to run at higher frequencies without sacrificing performance. The H cores are ideal for modern data-intensive applications like storage and networking.



Codasip Application Processors

The Application domain covers the most powerful cores with a RV64GC ISA and a complex pipeline (7 stages and above). The A cores were designed to support all the privilege modes and a memory management unit (MMU) needed to run Linux and other rich operating systems. Other features include integrated L1 Data and Instruction caches of configurable size, an internal interrupt controller, dynamic branch prediction, FPU, and on-chip debugger based on JTAG and RISC-V debug standards. These cores are suitable for applications that require an advanced user interface, sophisticated I/O and networking, such as in set-top boxes or entertainment systems; they can also support complex computations, full-process isolation and multitasking, or a full separation of application code from hardware via device drivers.



Features

Standard Buses

We provide native AMBA interface support for each processor. You can configure and customize the AHB-Lite or AXI-Lite interfaces, thus preserving your investments made in industry-standard peripheral IP blocks without taking the latency penalty that comes with using bus bridges.

Outstanding Software Infrastructure

Any Codasip core is supplied with an industry leading LLVM-based development environment that outperforms community alternatives across a wide range of benchmarks. This is because we have added proprietary optimizations to the LLVM back-end. For example, we introduced our own implementation of jump threading, a compiler pass that aims to speed up code execution by replacing conditional jumps with unconditional ones. With our implementation, we achieved up to 16.5% faster code compared to out-of-the-box LLVM jump threading.

Our standard development environment includes:

Hardware Development Kit (HDK)

- RTL (Verilog/VHDL/SystemVerilog)
- Verification report
- Integration test bench
- Sample EDA scripts

Codasip CodeSpace (Eclipse-based IDE)

Software Development Kit (SDK)

- C/C++ LLVM compiler (improved by Codasip)
- C/C++ Libraries (newlib)
- Assembler, disassembler, linker
- High-performance instruction set and cycle accurate simulators
- Debugger and profiler

Custom Features with Codasip Studio

If you use a Codasip core with Codasip Studio, you may not only choose among the standard extensions defined by the RISC-V specification, but you can innovate by creating your own custom instructions and changing microarchitectural features.

A Customer Example

Codasip user Microsemi was able to use Codasip Studio for exploring instructions for an audio application.

Results of extending a core with different instruction sets

Architecture	Cycles	Speedup vs. RV32I	Gatecount	Area vs. RV32I
RV32I	1,764 k		16.0k	
RV32I + serial multiplier	427k	× 4.12	19.7k	× 1.24
RV32I + parallel multiplier	133k	× 13.26	26.2k	× 1.64
RV32I + DSP extensions	31k	× 56.24	38.7k	× 2.43

Source: D. Ganousis & V. Subramaniam, Implementing RISC-V for IoT Applications, DAC 2017

They started with the RV32I base instruction set and found that their software took too many cycles to run. Adding a serial multiplier resulted in an incremental improvement, the parallel multiplier yielded a greater improvement for a cost in increased gatecount. However, custom DSP instructions resulted in a 56.24× improvement in cycle count for just a 2.43× greater gatecount. Codasip Studio was used to establish these tradeoffs in just days.

Automated Workflow

If you are adding value to a Codasip core in order to develop an innovative IC, the Codasip Studio toolset enables you to verify your modified core and then to automatically generate your HDK and SDK.

Debugging

Our embedded debug implementation combined with the Eclipse-based Codasip Studio (for processor customization) or Codasip CodeSpace (for software development) provides a unified experience from early architectural exploration to in-circuit FPGA and ASIC debug.

Codasip CodeSpace

Codasip CodeSpace is an advanced firmware development environment that enables you to write code for your new core. Codasip CodeSpace includes a code editor, compiler, profiler, and debugger. You will get a full 1-year license for free with any of our off-the-shelf RISC-V cores.

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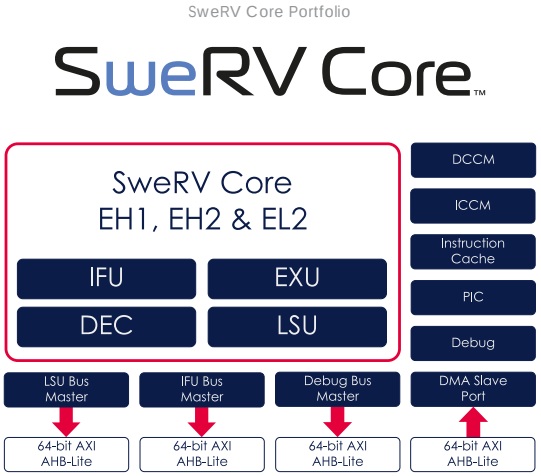
SweRV CORE SUPPORT PACKAGE

Open RISC-V Cores

Open-source cores may be an attractive option for using RISC-V, as the RTL has no license fee. But it is important that you factor in the total cost of the core ownership. To use the open-source RTL, you will need to set up a comprehensive hardware implementation and verification flow. You will also need software development tools. We offer all this within our exclusive **SweRV Core Support Package**.



SweRV Core EH1

The Western Digital SweRV Core™ EH1 is a 32-bit, two-way superscalar, 9-stage pipeline core. With a performance of up to 4.95 CoreMark/MHz and small footprint, it offers you compelling capabilities for embedded devices that support data-intensive edge applications such as storage controllers, industrial IoT, real-time analytics in surveillance systems, and other smart systems. The power efficient design also offers clock speeds greater than 800 MHz on a 28nm CMOS process technology.

SweRV Core EH2

The SweRV Core EH2 was derived from the EH1. It adds dual threaded capability for additional performance, which reaches outstanding 6.3 CoreMark/MHz.

SweRV Core EL2

The SweRV Core EL2 is a small, ultra-low-power core with moderate performance, optimized for applications such as state-machine sequencers and waveform generators. It was designed to replace state machines and other logic functions in SoCs.

The SweRV Cores will be used in Western Digital products in the coming years. The design is open to utilize and contribute to.

Enabling the Use of SweRV RISC-V Cores

With Codasip's exclusive SweRV Core Support Package, you can implement the SweRV Core™ into your chip at a fraction of the cost of competing technologies or creating your own EDA flows and software toolchain. We provide you with comprehensive support for popular 3rd party design tools, both open and commercial, that you can switch between easily. The Support Package covers hardware implementation and verification flow including scripts, simulation models and testbenches, embedded software development, emulation, implementation, and debug—everything you need to confidently deploy the core. Professional technical support is available too.

Package Configurations

We offer the SweRV Core Support Package in two configurations. The **Free package** consists of the Support Package infrastructure, an SDK including both command line and Eclipse CDT, software examples for both bare metal and FreeRTOS, and SweRV Core RTL.

The **Pro package** adds synthesis and simulation tools, static code analysis (linting), checkers for clock domain crossing and reset domain crossing, and RTL vs gate-level verification.

CORE CUSTOMIZATION

If you would like us to create a core to meet your requirements, get in touch with us.

On-request Service by Customization Experts

To create a fully custom core by yourself, you can use our powerful all-in-one customization toolset, **Codasip Studio**. With a familiar C-like description language and high level of automation, it makes the task easier than ever before.

If, however, you prefer to outsource the development, we are here to help as well: Please take advantage of **Codasip's customization services**. Our engineers can work with you to understand your requirements and to create your ideal processor core. This applies whether you would like to:

- Develop a custom version of a Codasip RISC-V Processors core
- Develop a custom SweRV core
- Develop a core using a special architecture (such as VLIW)

Choosing the Path to Your Ideal Core

At Codasip we appreciate that you will have unique requirements to meet the needs of your IC project. This is why we offer a number of routes providing you with the sort of core that best meets your needs.

There are not only different computational and cost requirements, but differing levels at which you may feel comfortable with customizing your own solution. Regardless of your requirements or abilities, we can find you a way to the core that you need.

PROVEN AGAIN AND AGAIN...

If you are looking for a processor solution for your SoC project, you want to be confident that you are building on a working and well-verified solution. Codasip's solutions whether using our cores, Codasip Studio or SweRV are silicon proven. We quote a few examples from around the world.

MYTHIC

Redwood City, USA
Mythic is a leader in artificial intelligence (AI) computing technology based on a unique approach to neural network processing.

Ty Garibay, VP of Hardware Engineering at Mythic

"Codasip gave us the flexibility to create a truly unique RISC-V processor, specific to our needs. This saved us the effort to build our own processor from scratch and allowed us to focus on other critical areas of the product development."

DONGWOON
(주)동운아나텍

Seoul, Korea
Dongwoon Anatech is a leader in analog and power ICs (integrated circuits) for mobile phones.

Jin Park, CTO of Dongwoon Anatech

"The RISC-V instruction set with custom DSP exten- sionsextensions delivers the performance we require while keeping silicon area to a minimum. The best-in-class Codasip Studio development tools enable us to profile our soft- ware and find an optimal set of instructions for our application."

...AND AGAIN

Rambus

Sunnyvale, California
Rambus is a leading provider of IP cores, software and services, specializing in performance and protection of data.

Bret Sewell, SVP and general manager of the Rambus Security Division

"Security is the leading issue for IoT, automotive and other fast-growing markets, and it is critical for Rambus to deliver superior products to market in a timely fashion. We selected Codasip Studio because it allows for fast design space exploration, and because of the high quality of results we are getting in the automatically generated compiler toolchain."

vidtoo 微迪兔

Hangzhou, China
Leader in semiconductor products for HPC (high-performance computing), artificial intelligence, and machine learning platforms.

Thomas Hu, CEO of Vidtoo Technologies

"After careful consideration, we determined that Codasip offered the best combination of performance, value and design expansion ability. Those traits, plus best-in-class support and the broad ecosystem that the open RISC-V ISA brings, gave us confidence that Codasip was the right choice."

ABOUT CODASIP

Company History

Codasip was founded in 2014 in the Czech Republic. Our technology is based on 10 years of prior university research at the Brno University of Technology/Faculty of Information Technology including the PhD theses of our CEO and CTO. After an initial funding round with Credo Ventures, Codasip completed a series A round with Ventech Capital, Western Digital, Shenzhen Capital Group, and Paua Ventures.

Codasip was a founding member of the RISC-V Foundation in 2015 and has actively contributed to their activities ever since. In the same year we also introduced our first RISC-V core to the market and have continued to extend our RISC-V product line.

Today, Codasip is a rapidly expanding business and a strong international player with sales representation all over the globe including Japan, Taiwan, Korea, India, and Israel.

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