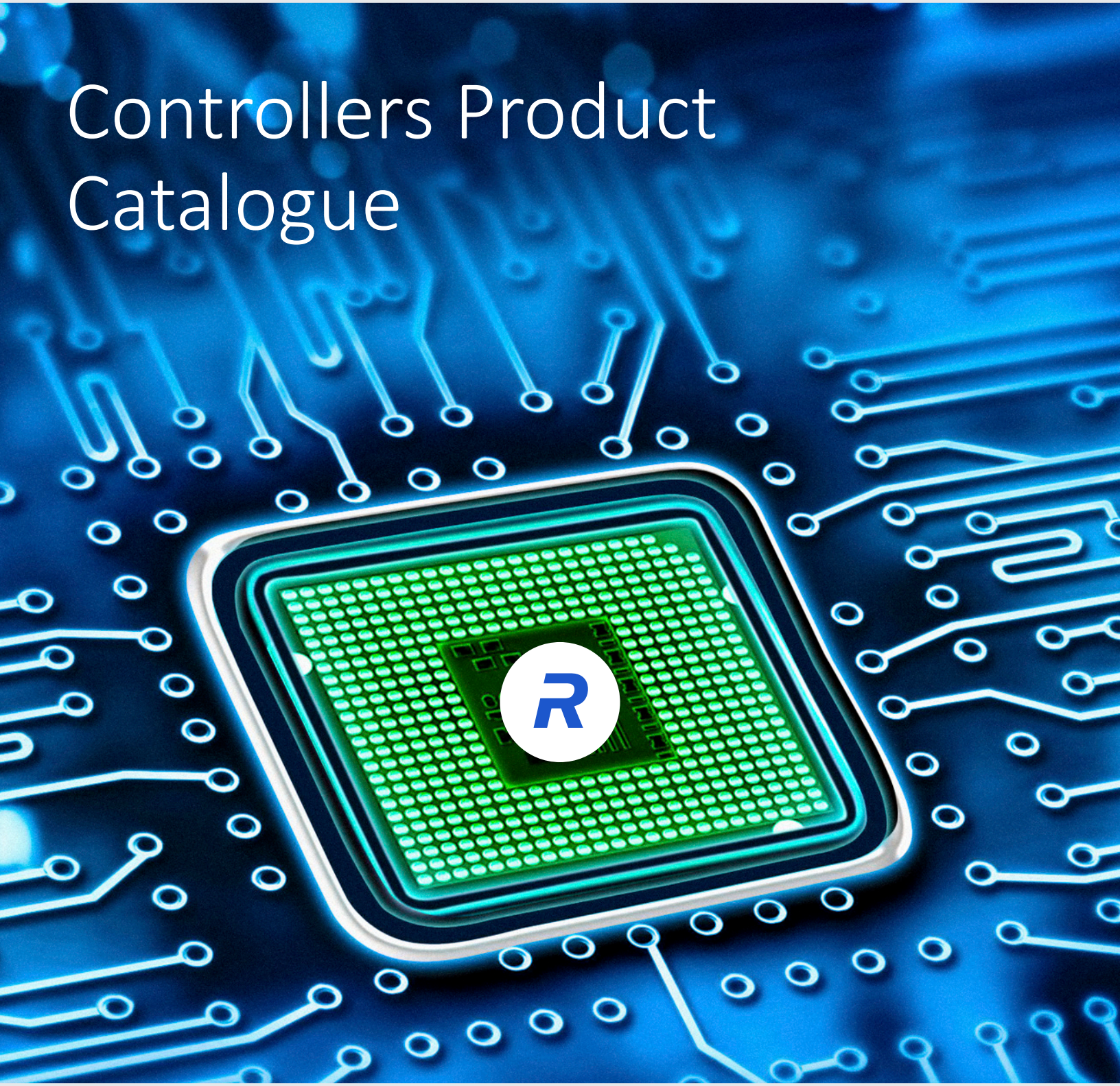
Controllers Product Catalogue



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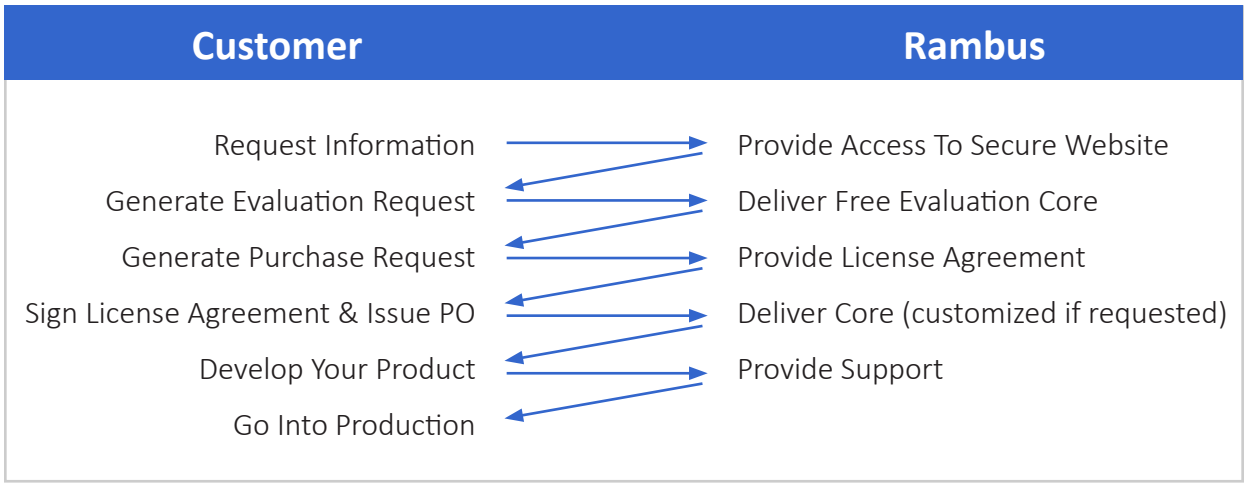
Memory Interface Solution

Overview

Rambus provides a broad range of IP Cores including PCI Express™, Memory Interface, MIPI, PCI and Peripheral cores. Key ad-vantages of Rambus IP Cores include:

- Silicon-proven, high-quality cores
- High performance – high throughput, high clock rate, low latency
- Easy to use- simple user interface, easy to configure, etc.
- Optimized for use in ASICs, Structured ASICs and FPGAs
- Fully hardware validated
- Provided with a testbench
- Development boards and driver support available
- Available as source code
- Core license includes expert technical support
- Customization and integration services available
- Widely used- references available

The Rambus standard delivery flow is show below:



As part of the evaluation process, Rambus encourages customers to have us review their requirements and system performance targets. We will then provide feedback as to whether our IP Cores can meet your requirements and point out potential system pitfalls. We also provide free evaluation cores for customers to further assess ease of integration and system throughput. Finally, we offer IP Core customization services to enhance a core to meet your specific needs.

For more information on Rambus and our IP Cores:
visit rambus.com/interface-ip/controllers/
or send an email to rcg@rambus.com

Frequently Asked Questions

1. **How do I get more information?**
   - Generate an Info Request using **rambus.com**, send an e-mail to **rcg@rambus.com**

2. **What happens after I request more information?**
   - You will be sent a password to access the secure web site. This site has a complete set of User Guides, Application Notes and Request Forms.

3. **How do I get pricing information?**
   - Generate a Pricing Request using the secure web site.

4. **How do I get a free evaluation core?**
   - Generate a Evaluation Request using the appropriate Request Form and e-mail it to rcg@rambus.com. You will receive the evaluation within two days.

5. **How is the evaluation core delivered?**
   - A structural netlist along with a Verilog testbench. Obfuscated source code is also available for potential ASIC customers. See the appropriate request form for more information.

6. **What are my purchase options?**
   - All IP Cores can be licensed as source code (ASIC and FPGA) or netlist (FPGA) for PCI Express and MIPI solutions
   - Memory Controller Cores are only available as source code (ASIC) and FPGA support is only available to ASIC customers doing FPGA prototyping

7. **How do I purchase a core?**
   - Generate a Purchase Request using the appropriate Request Form and e-mail it to **rcg@rambus.com**. You will then receive a filled-in License Agreement. Have it signed and issue a Purchase Order.

8. **How will the core be delivered?**
   - The core will be delivered via e-mail or using an FTP site.

9. **How do I get support?**
   - A senior support engineer will be responsible for handling all core delivery and support. They will supply a complete set of contact information along with the core delivery. If any questions arise, please contact them immediately via phone or e-mail.

10. **How much support is included?**
    - Rambus cores come standard with one year (ASIC) and six months (FPGA) of Maintenance & Support. Annual Maintenance & Support can be also purchased if desired.

11. **What does Maintenance & Support include?**
    - Unlimited phone & e-mail support, core maintenance releases and discounted upgrade pricing.

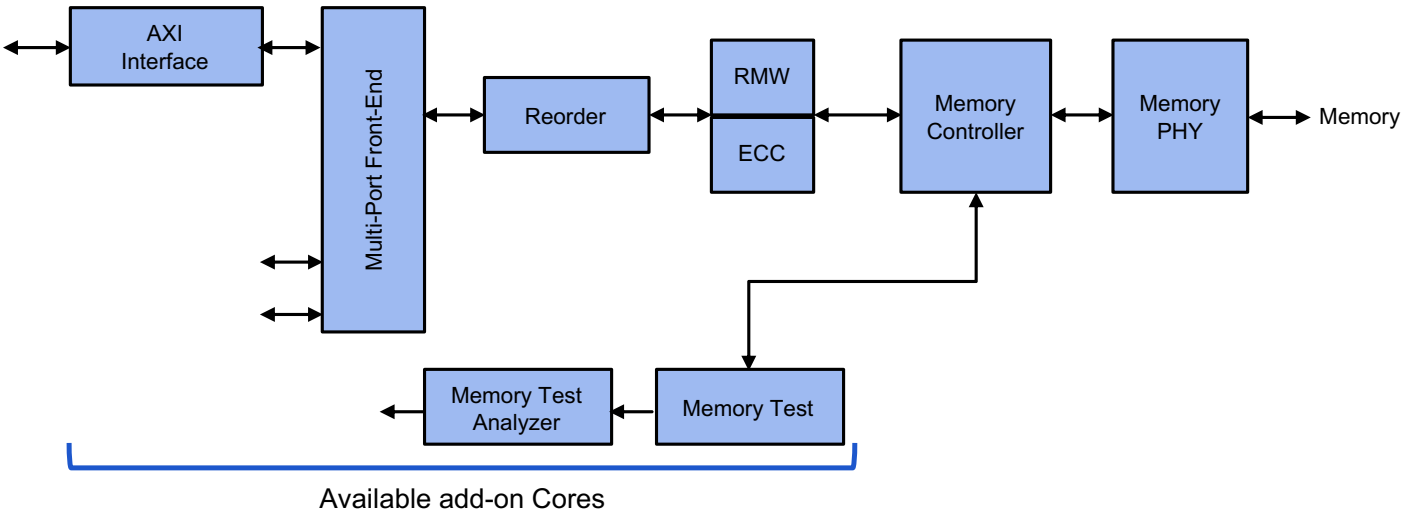
12. **Can I get a core with some custom features?**
    - Rambus is happy to customize a core to your requirements. Contact Rambus for a quote.

13. **What additional support can Rambus provide?**
    - Rambus provides IP Customization and Software Development services. Contact Rambus for a quote.

14. **Can I get some references?**
    - Rambus can provide a complete set of references upon request.

Rambus

Memory Interface Solution Overview



Solution Includes:

- **Memory Controller Cores**
  - Supports HBM2/2E, GDDR6, DDR4/3, LPDDR4
  - 64 banks and 16 deep command queue support
  - Supports all memory configurations including multi-rank, DIMM, RDIMM, LRDIMM etc.
  - Supports Full Rate, Half Rate and Quarter Rate operation
  - Provided with Memory Controller testbench
- **Add-On Cores**
  - Supports AXI Interfaces
  - Multi-port, priority-based arbitration support
  - Efficiency-based reordering maximizes memory utiliza-tion
  - Out-of-Band and In-Line ECC support
  - Comprehensive Memory Test Package supports chip and board bring-up
- **DDR PHY**
  - Fully integrated with a broad variety of third-party PHYs

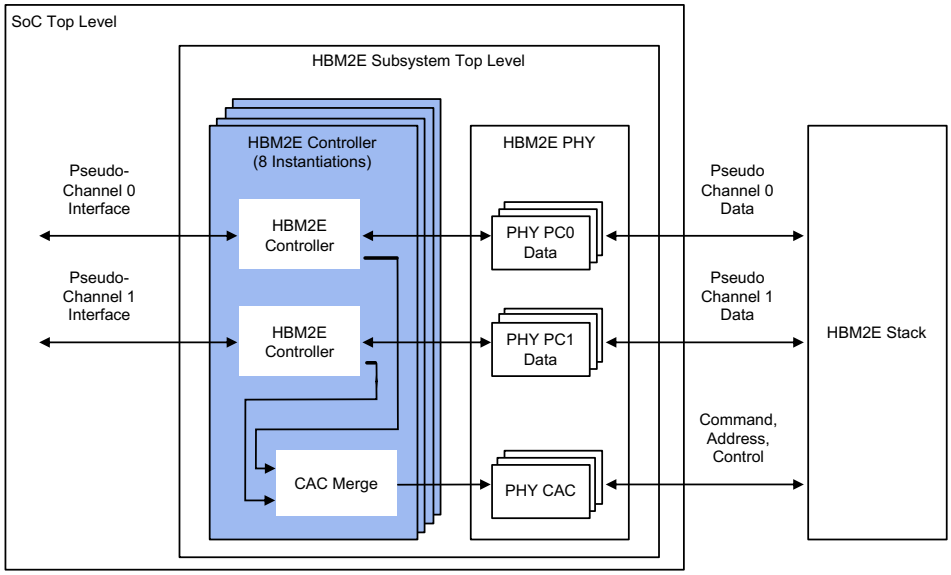
Key Features:

- **Complete Solution**
  - Full featured and modular solution enables IP to be configured to exact customer requirements
  - Flexible PHY interface supports all DFI compatible PHYs
  - Delivered fully integrated and verified with target DDR PHY
  - Minimal size relative to competition
  - JEDEC standard compliant
  - Silicon proven
- **High Performance**
  - Supports maximum data rates specified by the JEDEC standards
  - Supports high-efficiency, multi-port operation
  - Minimal latency
- **Easy-To-Use**
  - Simple interface, easy to configure, well-documented
- **Comprehensive Support**
  - ASIC, Structured ASIC and FPGA support
  - Expert technical support provided directly by designers
  - Integration and customization services available

HBM2/2E Controller Core

The Northwest Logic HBM2/2E controller core is designed for use in applications requiring high memory throughput including graphics, high performance computing (HPC), and artificial intelligence/machine learning (AI/ML).

HBM2E Dual-Controller Configuration



Overview

The Northwest Logic High Bandwidth Memory (HBM2E) Controller core from Rambus is designed for use in applications requiring high memory throughput, low latency and full programmability.

The core accepts commands using a simple local interface and translates them to the command sequences required by HBM2/2E devices. The core also performs all initialization, refresh and power-down functions.

The core queues up multiple commands in the command queue. This enables optimal bandwidth utilization for both short transfers to highly random address locations as well as longer transfers to contiguous address space. The command queue is also used to opportunistically perform look-ahead activates, precharges and auto-precharges, further improving overall throughput.

The core supports all HBM2/2E features, including: data bus inversion (DBI), DQ parity, command / address parity modes, and single-bank refresh. Add-On Cores such as a Multi-Port Front-End and Reorder Core can be optionally delivered with the core.

The core is delivered fully integrated and verified with the target HBM2/2E PHY.

Highlights

- Supports HBM2E and HBM2 devices
- Supports all standard HBM2E channel densities (4, 6, 8, 12, 16, 24 Gb)
- Supports up to 3.6 Gbps/pin
- Maximizes memory bandwidth and minimizes latency via Look-Ahead command processing
- Achieves high clock rates with minimal routing constraints
- DFI compatible (with extensions added for HBM2E)
- Supports AXI, or native interface to user logic

Protocol Compatibility

Standards	**Max Data Rates** (Gbps)
HBM2E	3.6 Gbps/pin

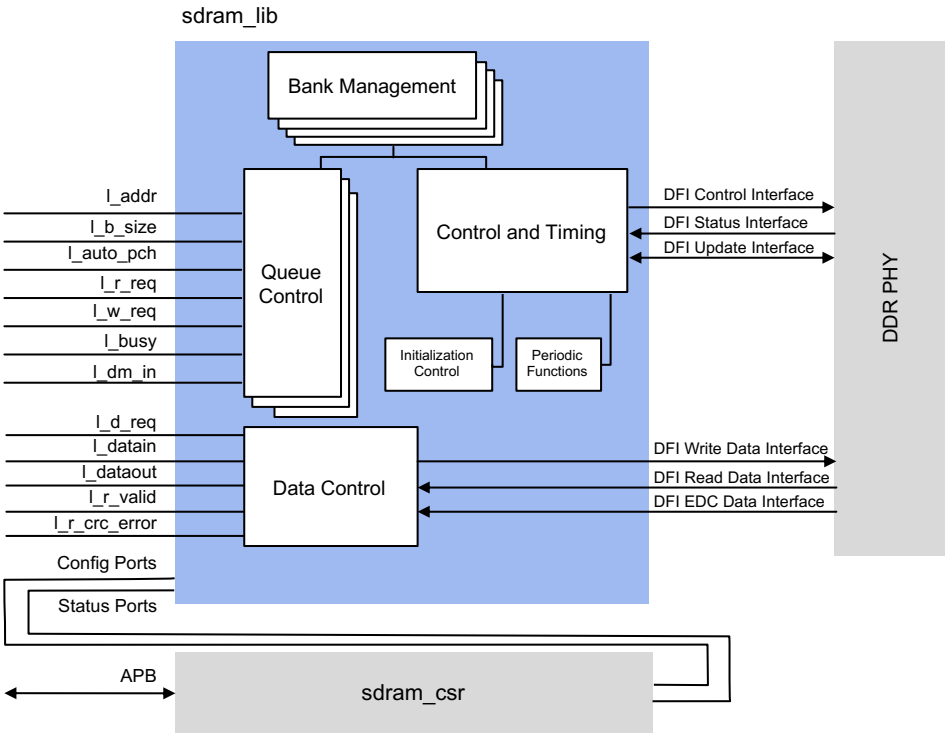
Deliverables

- Core (source code)
- Testbench (source code)
- Complete documentation
- Expert technical support
- Maintenance updates

GDDR6 Controller Core

The Northwest Logic GDDR6 controller core is designed for use in applications requiring high memory throughput including graphics, advanced driver assistance systems (ADAS), high performance computing (HPC), and artificial intelligence/ machine learning (AI/ML).

GDDR6 Controller Core Block Diagram



Highlights

- Up to 20 Gbps per pin operation
- Can handle two x16 channels
- Queue-based interface optimizes performance
- Maximizes memory bandwidth and minimizes latency via Look-Ahead command processing
- Supports clamshell mode
- DFI compatible
- Supports AXI or native interface to user logic

Protocol Compatibility

Standards	Data Rates (Gbps)
GDDR6	12, 14, 16, 18, 20

Deliverables

- Core (source code)
- Testbench (source code)
- Complete documentation
- Expert technical support
- Maintenance updates

Overview

The Northwest Logic GDDR6 Controller core from Rambus is designed for use in applications requiring high-memory throughput, high clock rates and full programmability.

The core accepts commands using a simple local interface and translates them to the command sequences required by GDDR6 SGRAM devices. The core also performs all initialization, re-fresh and power-down functions.

The core uses bank management techniques to monitor the status of each GDDR6 SGRAM bank (up to 16 banks managed concurrently). Banks are only opened or closed when necessary, minimizing access delays.

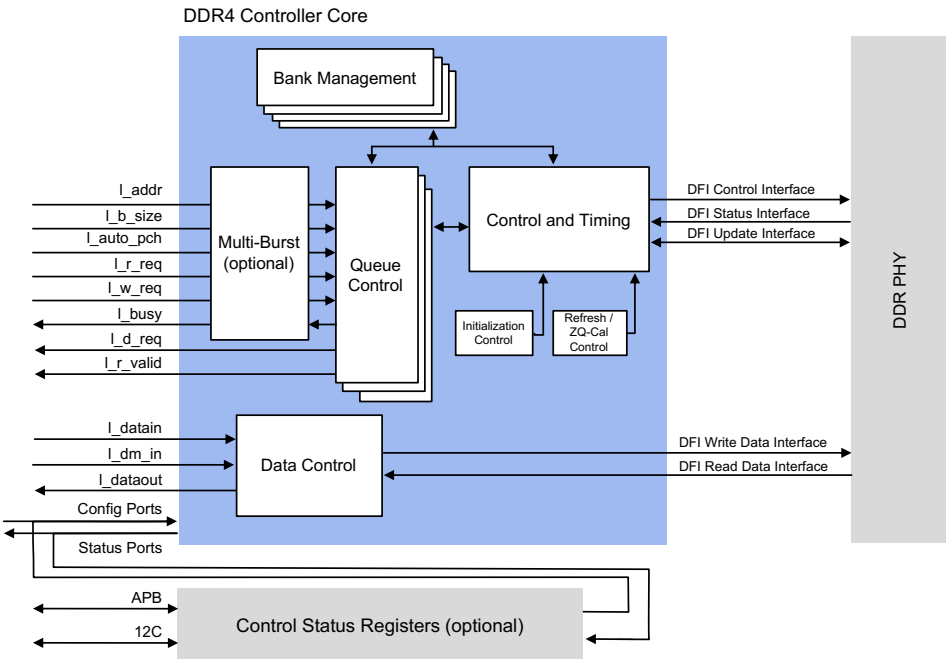
The core queues up multiple commands in the command queue. This enables optimal bandwidth utilization for both short transfers to highly random address locations as well as longer transfers to contiguous address space. The command queue is also used to opportunistically perform look-ahead activates, precharges and auto-precharges further improving overall throughput.

The core supports all GDDR6 SGRAM features, including: x16, x8 or x8 clamshell modes, error detection code (EDC), tracking of link error statistics, data bus inversion (DBI) and CA bus inversion (CABI).

DDR4 Controller Core

The Northwest Logic DDR4 controller core is designed for high memory throughput, high clock rates, and full programmability in computing and networking applications.

DDR4 Controller Core Block Diagram



Highlights

- Maximizes bus efficiency via look-ahead command processing, bank management, auto-precharge and additive latency support
- Supports half-rate and quarter-rate clock operation
- Supports DDR4 SDRAM 3DS device configurations
- DFI compatible
- RDIMM and LRDIMM support

Protocol Compatibility

Standards	**Data Rates** (Mbps)
DDR4	1600 to 3200

Deliverables

- Core (souce code)
- Testbench (source code)
- Complete documentation
- Expert technical support
- Maintenance updates

Overview

The Northwest Logic DDR4 Controller core from Rambus is designed for use in applications requiring high memory throughput, high clock rates and full programmability.

The core accepts commands using a simple local interface and translates them to the command sequences required by DDR4 SDRAM devices. The core also performs all initialization, refresh and power-down functions.

Bank management modules monitor the status of each SDRAM bank. Banks are only opened or closed when necessary, minimizing access delays. Up to 32 banks can be managed at one time.

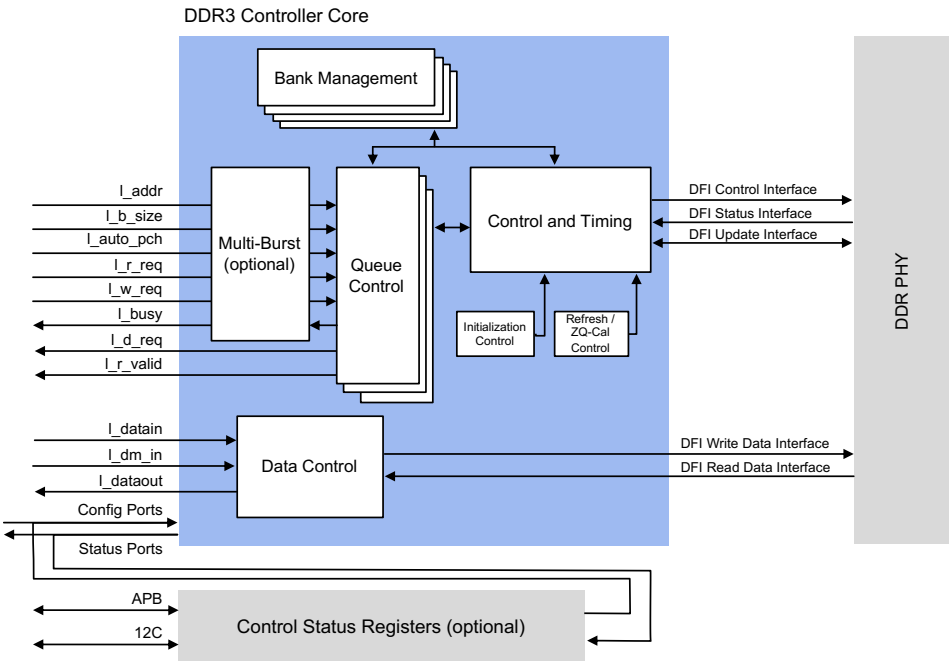
Multiple commands are queued enabling optimal bandwidth utilization for both short transfers to highly random address locations as well as longer transfers to contiguous address space. The command queue is also used to opportunistically perform look-ahead activates, precharges and auto-precharges further improving overall throughput.

The core supports all new DDR4 SDRAM features, including: 3DS device configurations, write CRC, data bus inversion (DBI), fine granularity refresh, additive latency, per-DRAM addressability, and temperature controlled refresh. Add-On cores such as a Multi-Port Front-End and Reorder core are available as options.

DDR3 Controller Core

The Northwest Logic DDR3 controller core is designed for high memory throughput, high clock rates, and full programmability in computing and networking applications.

DDR3 Controller Core Block Diagram



Highlights

- Maximizes bus efficiency via look-ahead command processing, bank management, auto-precharge and additive latency support
- Supports full-rate and half-rate clock operation
- Supports ODT, dynamic ODT, 2T timing and write leveling calibration
- DFI compatible
- Multi-mode controller support

Protocol Compatibility

Standards	**Data Rates** (Mbps)
DDR3	800 to 2133

Deliverables

- Core (source code)
- Testbench (source code)
- Complete documentation
- Expert technical support
- Maintenance updates

Overview

The Northwest Logic DDR3 Controller core from Rambus is designed for use in applications requiring high memory throughput, high clock rates and full programmability.

The core accepts commands using a simple local interface and translates them to the command sequences required by DDR3 SDRAM devices. The core also performs all initialization, refresh and power-down functions.

Bank management modules monitor the status of each SDRAM bank. Banks are only opened or closed when necessary, minimizing access delays. Up to 32 banks can be managed at one time.

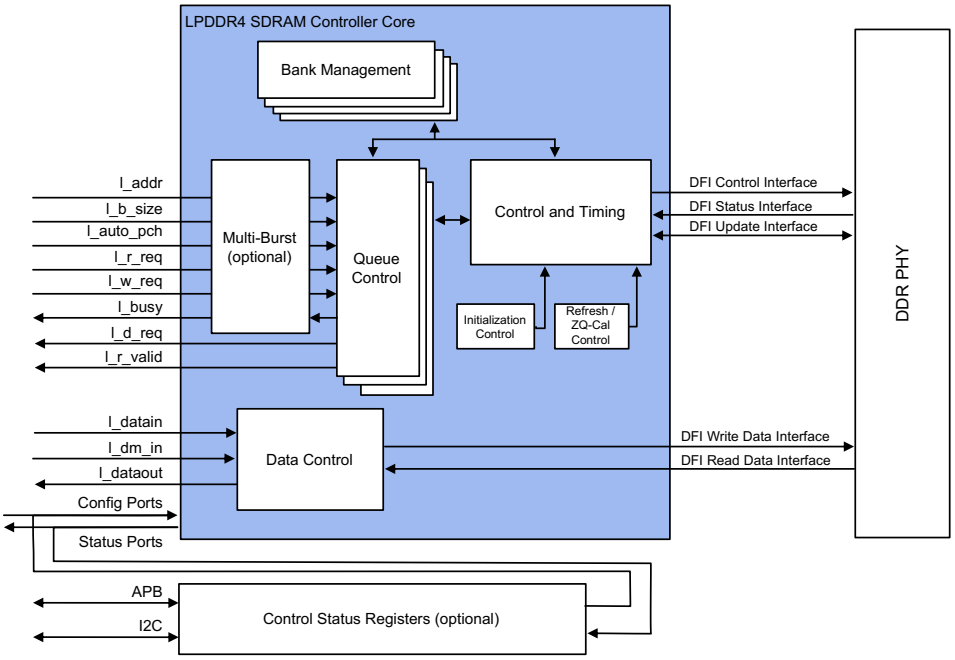
Multiple commands are queued enabling optimal bandwidth utilization for both short transfers to highly random address locations as well as longer transfers to contiguous address space. The command queue is also used to opportunistically perform look-ahead activates, precharges and auto-precharges further improving overall throughput.

The core is provided with run-time programmable inputs for all memory timing parameters and configuration settings. This ensures compatibility with all DDR3 SDRAM configurations. ODT, dynamic ODT, 2T timing and write leveling calibration are supported.

LPDDR4 Controller Core

The Northwest Logic LPDDR4 controller core is designed for use in applications requiring high memory throughput at low power including mobile, Internet of Things (IoT), automotive, laptop PCs, and edge networking devices.

LPDDR4 Controller Core Block Diagram



Highlights

- Maximizes bus efficiency via lookahead command processing, bank management, and auto-precharge
- Minimizes latency via parameterized pipeling
- Supports full-rate, half-rate and quarter-rate clock operation
- Supports LPDDR4 data bus inversion (DBI) and data mask (DM)
- Supports self-refresh, partial array self-refresh, power down, and deep power down modes

Protocol Compatibility

Standards	Data Rates (Gbps)
LPDDR4	3.2 Gbps/pin

Deliverables

- Core (source code)
- Testbench (source code)
- Complete documentation
- Expert technical support
- Maintenance updates

Overview

The Northwest Logic Low Power LPDDR4 Controller core from Rambus is designed for use in applications requiring high memory throughput, high clock rates and full programmability.

The core accepts commands using a simple local interface and translates them to the command sequences required by LPDDR4 devices. The core also performs all initialization, refresh and power-down functions.

The core uses bank management modules to monitor the status of each LPDDR bank. Banks are only opened or closed when necessary, minimizing access delays.

The core queues up multiple commands in the command queue. This enables optimal bandwidth utilization for both short transfers to highly random address locations as well as longer transfers to contiguous address space. The command queue is also used to opportunistically perform look-ahead activates, precharges and auto-precharges further improving overall throughput.

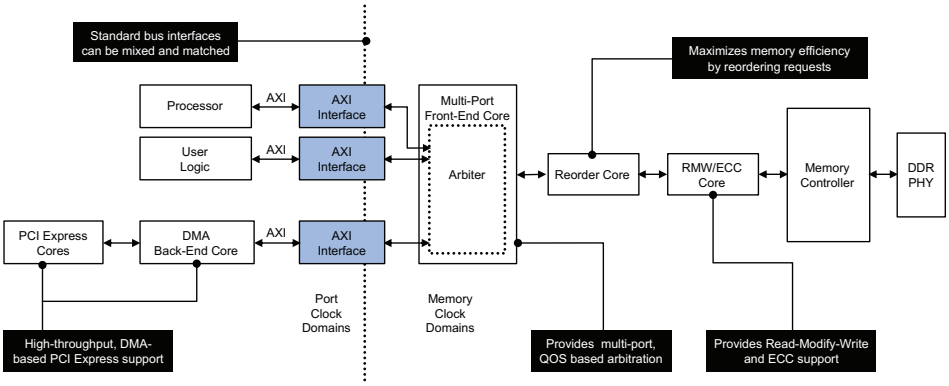
The core is provided with run-time programmable inputs for all memory timing parameters and configuration settings. This ensures compatibility with all LPDDR4 configurations.

Add-On cores such as a Multi-Port Front-End and Reorder core can be optionally delivered with the core. The core is delivered fully integrated and verified with the target DDR PHY.

AXI Interface Core

The Northwest Logic AXI Interface core is designed for use in applications requiring ARM's Advanced eXtensible Interface (AXI).

AXI Interface Core Application Example



Overview

The Northwest Logic AXI Interface core from Rambus is designed for use in applications requiring ARM's Advanced eXtensible Interface (AXI).

The core accepts write and read requests from a Bus Master. After receiving a write request the core immediately accepts the associated write data enabling the Bus Master to proceed to the next request. The core then arranges for the data to be written into the memory. After receiving a read request, the core arranges for the data to be read from the memory and then provides it to the Bus Master.

The core handles the conversion of the bus width/speed to the memory width/speed. This enables the bus width and speed to be completely independent of the memory width and speed. The core can be used in a single port configuration connected directly to the Memory Controller core. Multiple instances of the core can be used with the Northwest Logic Multi-Port FrontEnd core. This enables a multi-port design with a mix of different types of bus interfaces to be quickly and easily created.

Rambus also provides the AXI Interface core with a testbench which serves as a bus functional model.

The AXI Interface core requires the Read-Modify-Write core which is licensed separately.

Rambus also provides IP Core customization services.

Highlights

- Provides high-performance interface to AXI
- Handles conversion of bus width/ speed to memory width/speed
- Provided with a bus functional model (testbench)
- Achieves high clock rates with minimal routing contrstraints
- Source code available
- Customization and integration services available

Deliverables

- Core (source code)
- Testbench (source code)
- Complete documentation
- Expert technical support
- Maintenance updates

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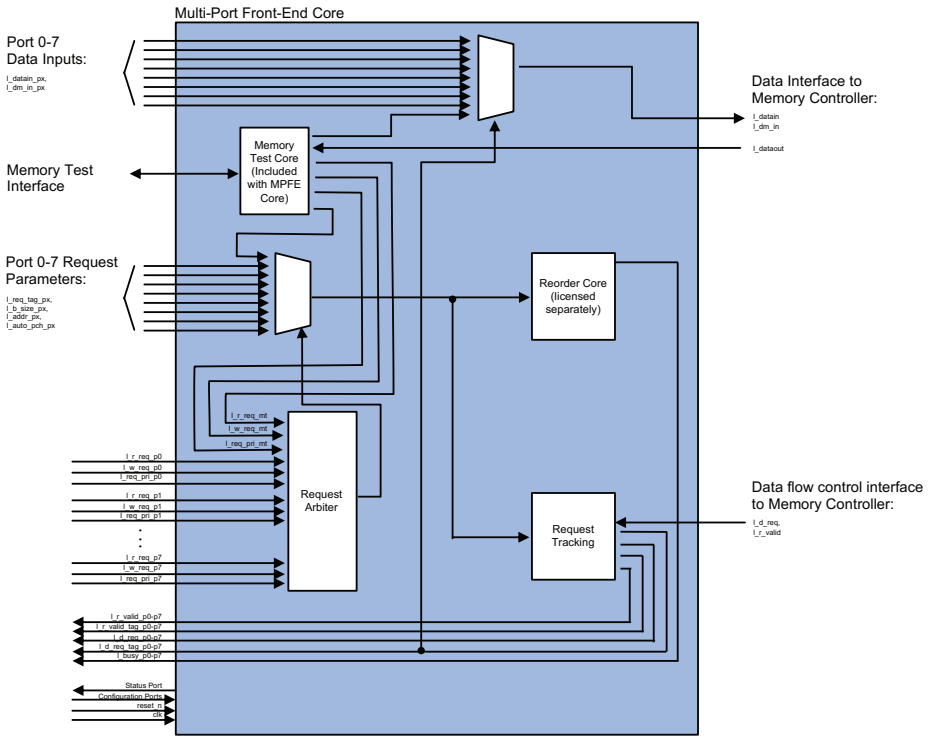
Multi-Port Front-End Core

The Northwest Logic Multi-Port Front-End core provides a multi-port interface to Northwest Logic Memory Controller cores.

Multi-Port Front-End Block Diagram



Highlights

- Provides a multi-port interface to Memory Controller cores
- Supports up to 8 user ports
- Prevents request stalling using request timeout
- Achieves high clock rates with minimal routing constraints
- Minimal ASIC gate count
- Source code available
- Customization and integration services available

Deliverables

- Core (source code)
- Testbench (source code)
- Complete documentation
- Expert technical support
- Maintenance updates

Overview

The Northwest Logic's Multi-Port Front-End core from Rambus provides a multi-port interface to the Northwest Logic Memory Controller cores.

Each user request is provided with its own request priority.
The arbiter selects requests based on priority and then round robin arbitration. Each port also has a programmable time out period. A timed-out request is given highest level priority ensuring its quick execution.

Rambus also provides IP core customization services.

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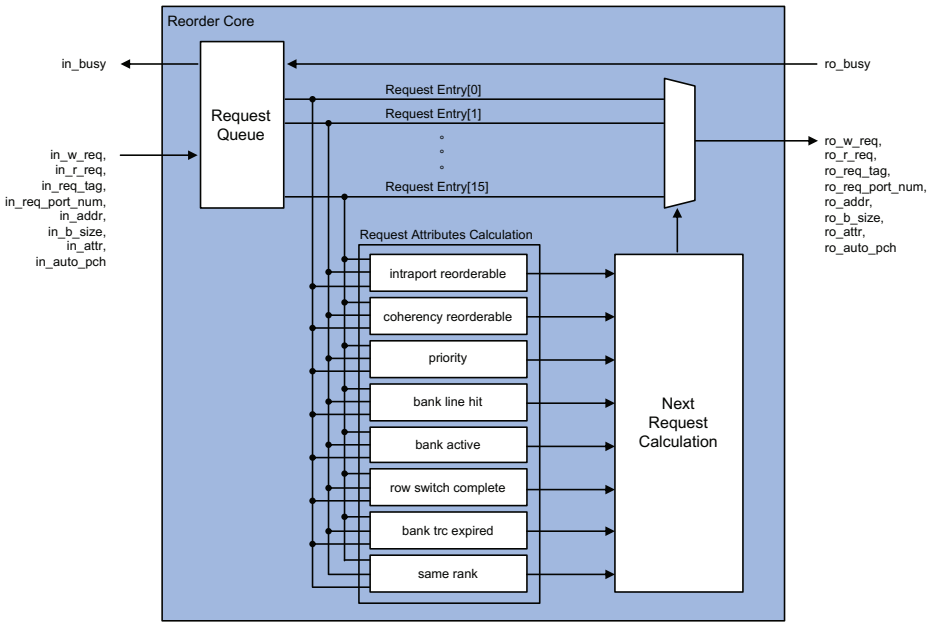
Reorder Core

The Reorder core reorders requests based first on priority and second on throughput optimization.

Reorder Core Block Diagram



Highlights

- Reorders requests based on priority and throughput optimization
- Can be used in single port or multi-port configurations
- Option to enforce data coherency during reordering operation
- Option to enable/disable intraport reordering
- Reorder queue bypassed when empty to minimize latency
- Achieves high clock rates with minimal routing contrstraints
- Source code available
- Customization and integration services available

Deliverables

- Core (source code)
- Testbench (source code)
- Complete documentation
- Expert technical support
- Maintenance updates

Overview

The Northwest Logic Reorder core from Rambus reorders requests based first on priority and second on throughput optimization.

Throughput optimization includes moving same bank/same row requests next to each other, same bank/different row requests away from each other, moving reads next to reads and writes next to writes.

The core can be used to optionally enforce data coherency by preventing any same row requests from passing over each other.

The core can also optionally disable intra-port (within a port) reordering. Disabling intra-port reordering ensures that the requests on each port are always executed in the same order. In this case, only inter-port (between ports) reordering is allowed. The core can be used in single port or multi-port mode in conjunction with the Northwest Logic Multi-Port FrontEnd core.

To minimize latency, the core's reorder queue is bypassed when empty. This enables requests to flow directly through the core when no outstanding requests have been queued up.

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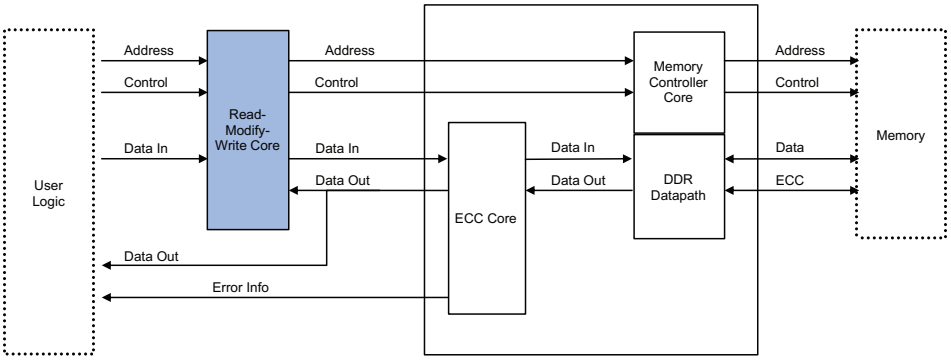
Read-Modify-Write Core

The Northwest Logic Read-Modify-Write (RMW) core handles misaligned bursts when an Error Correction Code (ECC) is being used.

Read-Modify-Write Core Application Example



Overview

The Northwest Logic Read-Modify-Write (RMW) core from Rambus handles misaligned bursts when an Error Correction Code (ECC) is being used.

An ECC code word must be calculated over an entire data word. Misaligned bursts can have partial data words at the front and back end of the burst. To calculate the correct ECC code word, the Read-Modify-Write core forms the correct starting and ending data words by reading the existing data words and combining them appropriately with the new partial data words.

The core performs address translation from byte addressing to the 64-bit or 128-bit addressing of the memory devices. The core is provided with the Multi-Burst core enabling it to automatically break long burst requests into multiple requests matching the memory's native burst length.

Read-Modify-Write write operations are by their very nature inefficient. The Read-Modify-Write core implements a prefetch architecture that maximizes the memory bus utilization as efficiently as possible.

The core is compatible with memory modules that don't provide Data Mask lines.

Rambus also provides IP core customization services.

Highlights

- Performs RMW operations at the start and end of misaligned burst writes when using ECC
- Performs translation from byte addressing to 64-bit or 128-bit addressing of the memory devices
- Automatically breaks long burst requests into multiple requests matching the memory's native burst length
- Prefetch architecture maximizes memory bus efficiency
- Simple user interface signaling
- Minimal ASIC gate count
- Source code available
- Customization and integration services available

Deliverables

- Core (source code)
- Testbench (source code)
- Complete documentation
- Expert technical support
- Maintenance updates

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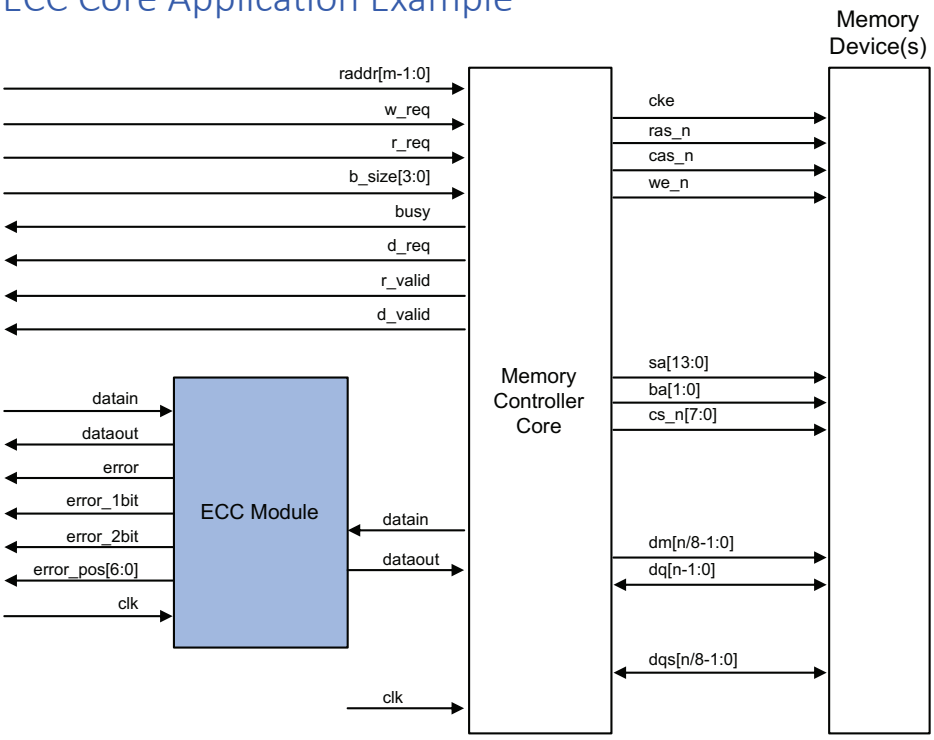
ECC Core

The Northwest Logic Error Correction Coding (ECC) core implements the standard Hamming Code-based DRAM Single Error Correction (SEC) and Double Error Detection (DED) algorithm.

ECC Core Application Example



Highlights

- Implements standard DRAM Single Error Correction (SEC) and Double Error Detection (DED) algorithm
- Generates an 8-bit ECC word for a 64-bit data bus
- Error flags indicate what type of error occurred (1-bit or 2-bit)
- Bit position of the error is provided for single-bit errors
- Supports ECC scrubbing
- Minimal ASIC gate count
- Source code available
- Customization and integration services available

Deliverables

- Core (source code)
- Testbench (source code)
- Complete documentation
- Expert technical support
- Maintenance updates

Overview

The Northwest Logic's Error Correction Coding (ECC) core from Rambus implements the standard Hamming Code-based DRAM Single Error Correction (SEC) and Double Error Detection (DED) algorithm. This algorithm generates an 8-bit ECC word for a 64-bit data bus.

The core consists of an ECC generation path as well as ECC detection and correction. ECC correction is possible for single bit errors occurring in one of combined 72 data and check bits. ECC detection is possible for errors in two of the combined 72 data and check bits.

Various status information is provided to the user including whether an error was detected on a single bit or two bits. The bit position of the error is provided for the case of a single bit errors. The Read-Modify-Write (RMW) core can be used in conjunction with the ECC Core when dealing with misaligned bursts. An ECC code word must be calculated over an entire data word. Misaligned bursts can have partial data words at the front and back end of the burst.

To calculate the correct ECC code word, the Read-Modify-Write Core forms the correct starting and ending data words by reading the existing data words and combining them appropriately with the new partial data words.

Rambus also provides IP Core customization services.

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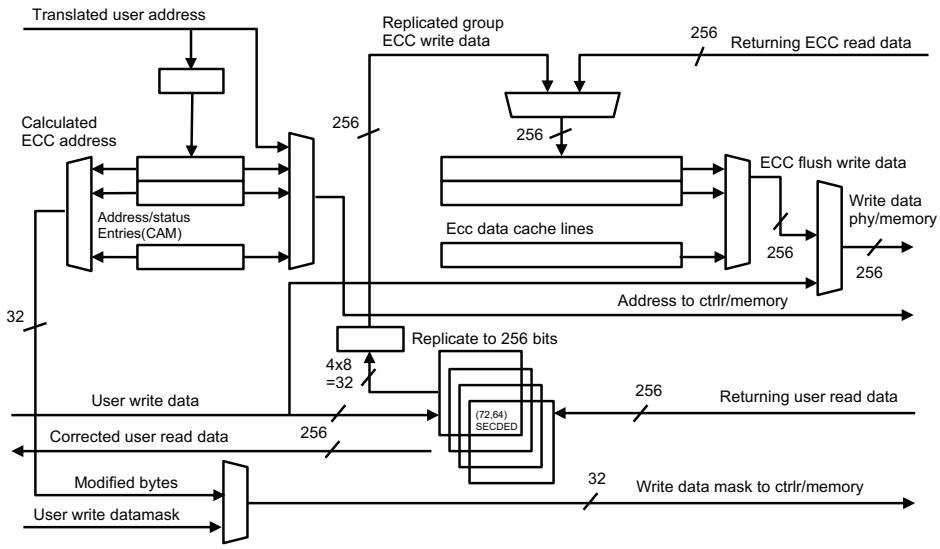
In-Line ECC Core

The Northwest Logic In-Line Error Correction Coding (ECC) core implements standard DRAM Single Error Correction (SEC) and Double Error Detection (DED) algorithm.

In-Line ECC Core Block Diagram



Highlights

- Supports Northwest Logic GDDR6 and LPDDR4 Controller cores
- Implements standard DRAM Single Error Correction (SEC) and Double Error Detection (DED) algorithm
- Generates an 8-bit ECC word for each 64 bits of data
- Error flags indicate what type of error occurred (1-bit or 2-bit)
- Bit position of the error is provided for single-bit errors
- Optimally only 1 ECC access is needed to support up to 8 data reads or 8 data writes (88.9% of data bandwidth)

Deliverables

- Core (source code)
- Testbench (source code)
- Complete documentation
- Expert technical support
- Maintenance updates

Overview

The Northwest Logic In-Line Error Correction Coding (In-Line ECC) core from Rambus works with the Northwest Logic GDDR6 and LPDDR4 Controller cores. The In-Line ECC implements the standard Hamming Code-based DRAM Single Error Correction (SEC) and Double Error Detection (DED) algorithm. This algorithm generates an 8-bit ECC value for each 64 bits of data.

Since GDDR6 memory does not support “out-of-band” ECC data protection efficiently, the In-Line ECC core provides the option to use 11.1% of the GDDR6 data memory to hold ECC bytes that protect the remaining 88.9% of data. In-line ECC thus consumes some of the available bandwidth to provide data protection. The same applies for an LPDDR4 implementation.

The core consists of an ECC generation path as well as ECC detection and correction. ECC correction is possible for single-bit errors occurring in one of the combined 72 data and check bits. ECC detection is possible for errors in two of the combined 72 data and check bits.

Various status information is provided to the user including whether an error was detected on a single bit or two bits. The bit position of the error is provided for the case of a single bit error. ECC check bytes are distributed throughout memory in “groups” to allow accesses to normally occur to the same row, bank pair (page) as the user data access that it protects.

To optimize performance, when using the Reorder core or Multi-Port Front-End core, the In-Line ECC core is placed between the GDDR6 (or LPDDR4) controller and the aforementioned cores. This minimizes the amount of ECC data caching that is needed. When not using the Reorder or Multi-Port Front End cores, the In-line ECC core is placed between the user interface and the GDDR6 (or LPDDR4) controller.

Rambus also provides IP core customization services.

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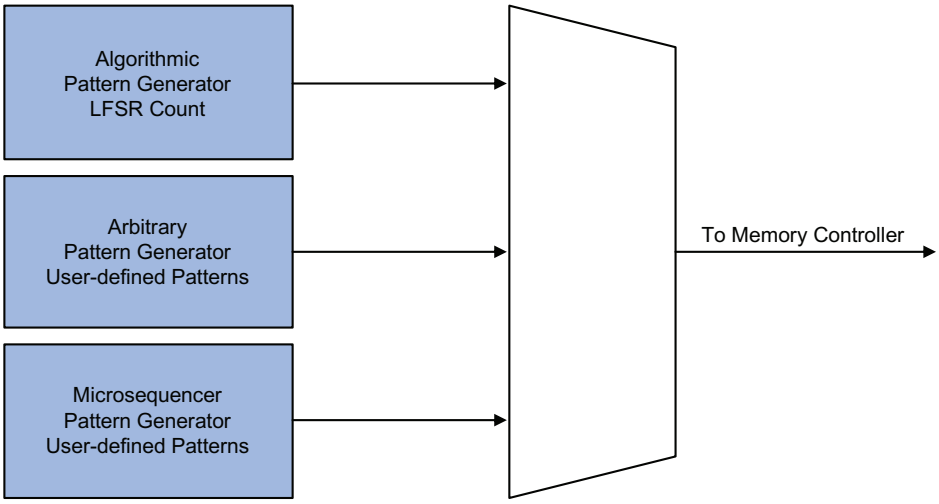
Memory Test Core

The Memory Test core provides comprehensive memory test support for chip and board verification.

Memory Test Core Block Diagram



Overview

The Northwest Logic Memory Test core from Rambus provides comprehensive memory test support for chip and board validation.

The base version of the core supports walking ones and zeroes, counting, random, and user programmable data patterns. It also supports sequential, random and user programmable address patterns. The random address and data pattern is particularly useful because it can fully stress both the chip and board design.

The Mem Test Analyzer core can be used in conjunction with the Memory Test core to capture the actual and expected test data.

The advanced memory test (AMT) option adds a microsequencer to efficiently generate complex memory test patterns such as MARCH, MATS+, GALPAT, and MOVI. These patterns can be used to isolate memory failures.

AMT is particularly useful for HBM-based memory systems. It includes support for HBM single-bank refresh control, synchronized test execution and parallel memory test RAM loading.

The AMT is provided with example test sequences and an assembler. Users can easily create custom test sequences that can be efficiently executed in the bring-up lab, manufacturing or in field test scenarios.

Highlights

- Part of a comprehensive memory test package with test support for chip and board validation
- Supports walking ones and zeroes, counting and user programmable patterns
- Supports sequential, random and user programmable address patterns
- Advanced memory test support
- Minimal ASIC gate count
- Pipelined design enables timing closure at high clock rates
- Customization and integration services available

Deliverables

- Core (source code)
- Testbench (source code)
- Complete documentation
- Expert technical support
- Maintenance updates

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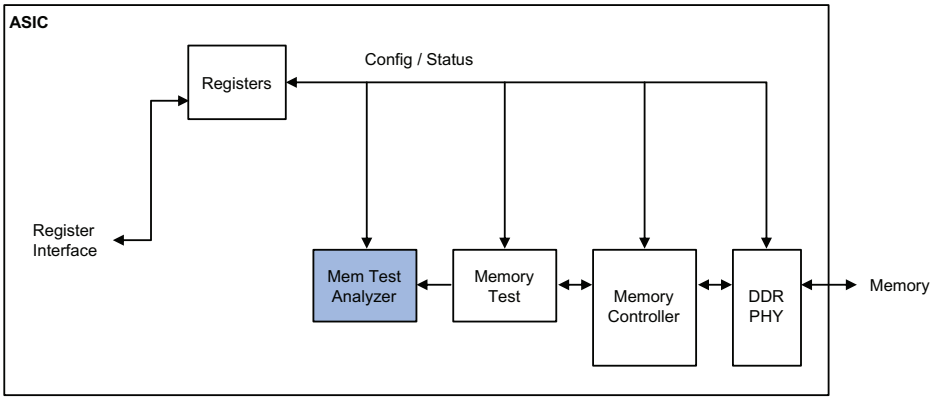
Mem Test Analyzer Core

The Northwest Logic Mem Test Analyzer core is used to capture the results from the Northwest Logic Memory Test core.

Mem Test Analyzer Core Application Example



Overview

The Northwest Logic Mem Test Analyzer Core from Rambus is used to capture the results from the Northwest Logic Memory Test core.

The Mem Test Analyzer core can be used in conjunction with the Memory Test core to capture the actual and expected test data. The capture is initiated by an error trigger signal provided by the Memory Test core. This data can then be retrieved from the Mem Test Analyzer core via the chip's configuration and status bus, on-chip processor or dedicated low-pin count serial port.

The core is useful for chip and board validation. It provides low-cost, built-in logic analyzer capability similar in concept to the FPGA-based internal logic analyzer tools.

Rambus also provides IP core customization services.

Highlights

- Part of comprehensive memory test package
- Capture results from Northwest Logic Memory Test core
- Data retrieved via chip's configuration and status bus, on-chip processor or dedicated low pin-count serial port
- Easy-to-use software including scripts and driver included
- Provides low-cost, built-in logic analyzer capability
- Useful for chip and board validation
- Minimal ASIC gate count
- Source code available
- Customization and integration services available

Deliverables

- Core (source code)
- Testbench (source code)
- Complete documentation
- Expert technical support
- Maintenance updates

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Rambus

Memory Interface Solution – FAQ

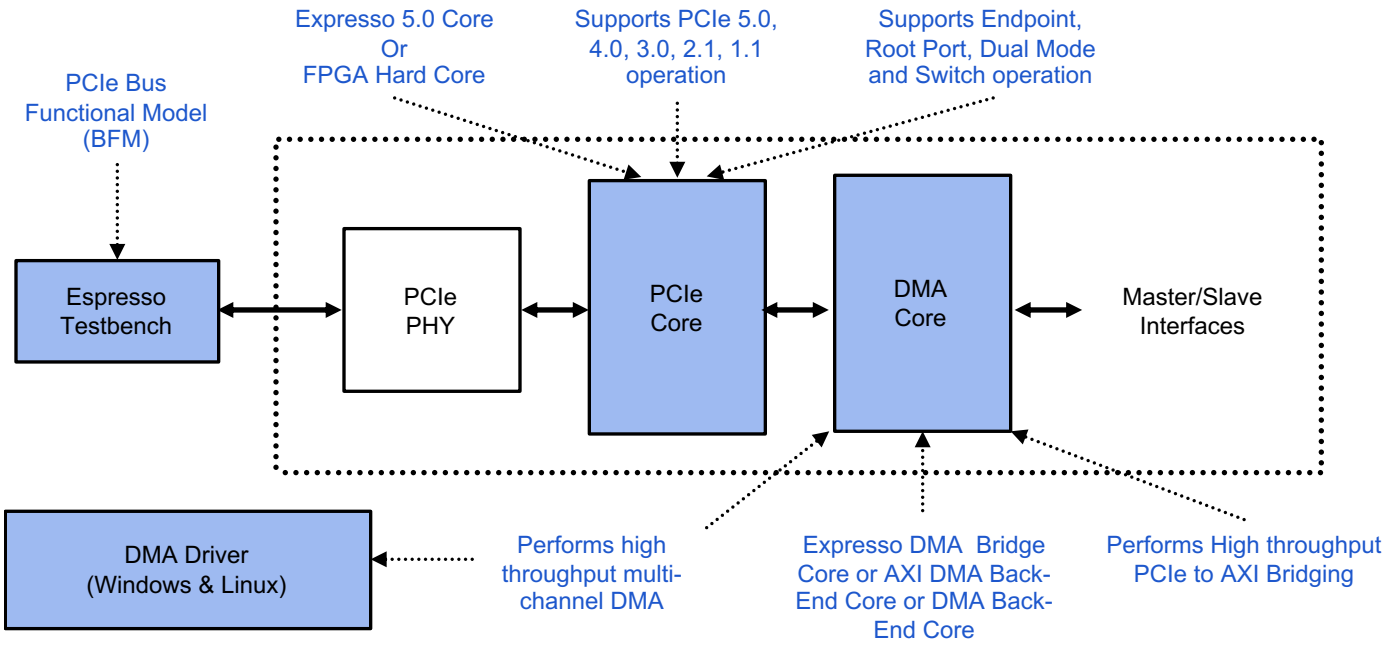
1. **What differentiates Rambus Memory Interface Solution from other vendor's cores?**
   - Complete solution- Handles all design, test and bring-up challenges
   - Supports broad range of memory types and configurations
   - High-bus efficiency- The cores employ all of the techniques available to achieve maximum throughput including request reordering, look-ahead command processing, bank management and auto-precharge.
   - Minimal latency- The cores have parameterized pipelining. This enables the cores to have a minimal latency when used in an ASIC while using the pipelining to achieve speed in an FPGA.
   - High data rates- Supports 4,267+ Mbit/s (ASIC), 1,867 Mbit/s (FPGA)
   - Small size- The cores are significantly smaller than other ASIC offerings.
   - Full set of optional add-on modules- Enables designer to choose the pieces that are needed for a particular design
   - Ease-of-Use- The cores have a very simple interface, require minimal constraints and are uniquely optimized for each device family.
   - Run-time programmability- All parameters including row/column configuration are run-time programmable.
   - Usable in both FPGAs and ASICs- Allows a design to be prototyped in an FPGA before creating the ASIC.
   - Comprehensive DDR PHY support
   - Provided with complete Testbench
   - Source code available
   - Expert Support- Fast turnaround support is provided by the actual designers.
   - Customization & Integration Services- Rambus is available to customize the cores to meet your unique needs and integrate the cores with additional logic.

2. **Can I use the Memory Interface Solution in an ASIC?**
   - Rambus delivers the solution pre-configured for use in an ASIC. This includes integration and verification with the target DDR PHY.
   - Rambus supports a broad range of DDR PHYs. Contact Rambus for more information.
   - Rambus Memory Interface Solution has been used in a variety of different ASIC designs. Contact Rambus for more information.

3. **Can I use the Memory Interface Solution in an FPGA?**
   - Memory Controller FPGA support is only available to ASIC customers doing FPGA prototyping
   - Rambus Memory Interface Solution Cores are specifically designed to achieve the maximum possible performance in programmable logic with a minimum number of constraints. This is achieved by minimizing the amount of logic and careful use of pipelining.
   - Rambus supports a wide variety of FPGA-based boards which can be used to prototype a design including Rambus Memory Interface Solution. Contact Rambus for more information.

Rambus

PCI Express Solution Overview



Solution Includes:

- **Expresso Cores**
  - PCI Express 5.0, 4.0, 3.0, 2.1 and 1.1 support
  - x16, x8, x4, x2, x1 including bifurcation support
  - Endpoint, Root Port, Dual Port & Switch support
  - Multi-Function and SR-IOV support
- **DMA Cores**
  - High-performance, multi-channel, scatter-gather DMA operation
  - FIFO and Memory mapped DMA support
  - Supports host-based and local descriptors
  - AXI4/3 Interface support
  - Support Rambus soft cores and FPGA hard cores

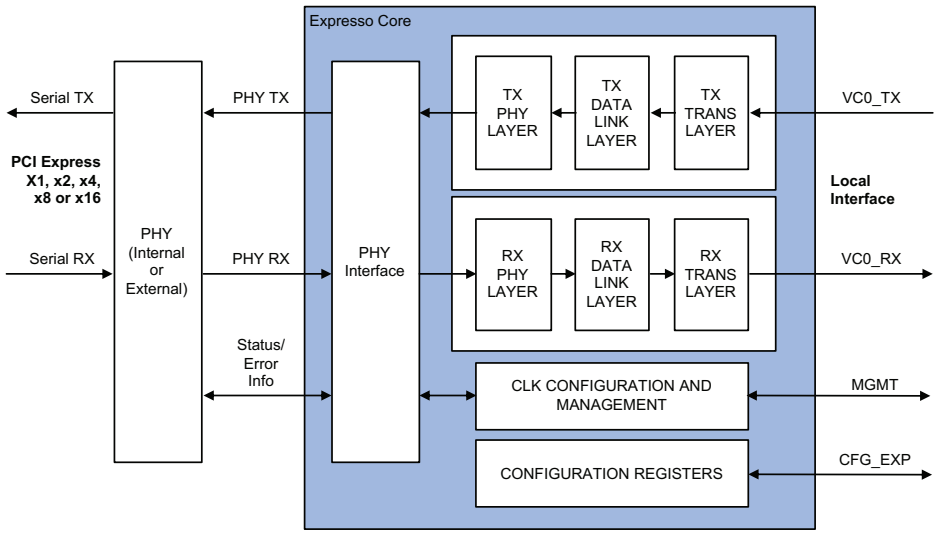
Key Features:

- **Complete Solution**
  - Includes complete PCIe and DMA support
  - Flexible PHY interface supports all PIPE compatible PHYs
  - Delivered fully integrated and verified with target PCIe PHY
  - PCIe standard compliant and PCI-SIG certified
  - Silicon proven
- **High Performance**
  - Supports full-duplex, scatter-gather DMA operation
  - Supports high-performance PCIe-AXI bridging
  - Provides maximum bandwidth across a wide range of applications
- **Easy-To-Use**
  - Simple interface, easy to configure, well-documented
- **Comprehensive Support**
  - ASIC, Structured ASIC and FPGA support
  - Expert technical support provided directly by designers
  - Integration and customization services available

Expresso 5.0 Core

The Northwest Logic Expresso 5.0 core is designed for maximum performance and ease of use for PCI Express® (PCIe) 5.0 applications. It is backwards compatible with PCIe 4/3/2/1 specifications.

Expresso 5.0 Block Diagram



Highlights

- x16, x8, x4, x2, x1 lane support
- 1-8 Physical Function support
- SR-IOV support up to 255 Virtual Functions
- Endpoint, Root Port, Upstream Switch Port, Downstream Switch Port, Bifurcation support
- 32, 64, 128, 256 and 512-bit core width support
- Full Transaction Layer (TL), Partial TL and TL Bypass interface options available
- Flexible equalization algorithms

Protocol Compatibility

Standards	Data Rates (Gbps)
PCIe 5.0	32, 16, 8, 5, 2.5

Deliverables

- Core (source code)
- Testbench (source code)
- Complete documentation
- Expert technical support
- Maintenance updates

Overview

The Northwest Logic Expresso 5.0 core from Rambus is designed for maximum performance and ease of use for PCIe 5.0 applications. It is backwards compatible with PCIe 4/3/2/1 specifications.

The Expresso 5.0 Core separately, or in combination with the Northwest Logic family of DMA cores and DMA drivers, provides the maximum system throughput on a PCIe link.

The core is specifically designed for ease of use including full receive packet decoding, complete error handling, automatic handling of PCIe message packets and comprehensive system-debug and link monitoring support.

The core is delivered integrated and verified with the user's target PHY. A complete list of supported PHYs is available on request. To accelerate simulations, the core is also delivered integrated with a fast-simulating behavioral PHY.

The core is provided with the Expresso Testbench which provides a PCIe Bus Functional Model.

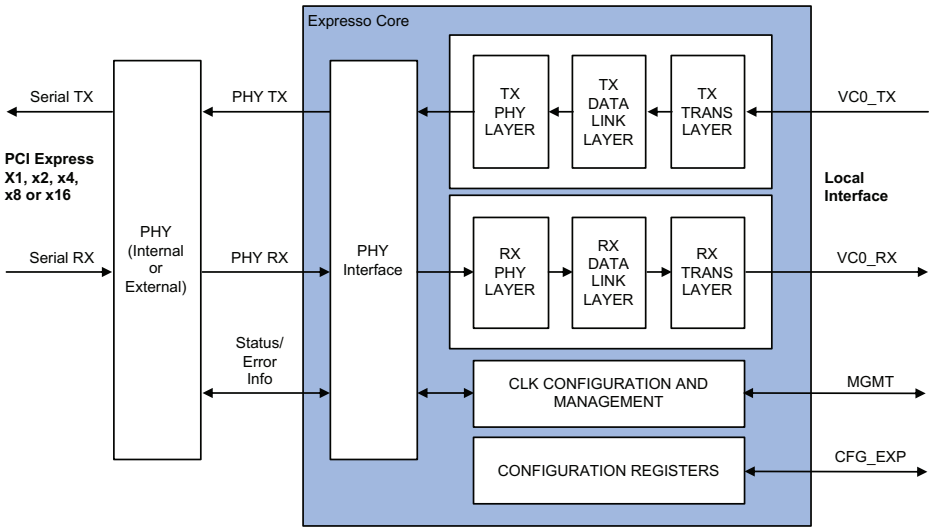
The core is compliant with the current version of the PCIe Base Specification 5.0. The core has been extensively validated with the Avery Design Systems PCI-Xactor PCIe Compliance Suite and Northwest Logic Expresso Testbench.

IP Core customization services are also available.

Expresso 4.0 Core

The Northwest Logic Expresso 4.0 core is designed for maximum performance and ease of use for PCI Express (PCIe) 4.0 applications. It is backwards compatible with PCIe 3.0/2.1/1.1 specifications.

Expresso 4.0 Block Diagram



Highlights

- x16, x8, x4, x2, x1 lane support
- 1-8 Physical Function support
- SR-IOV support up to 255 Virtual Functions
- Endpoint, Root Port, Upstream Switch Port, Downstream Switch Port, Bifurcation support
- 32, 64, 128 and 256-bit core width support
- Transaction Layer (TL), Partial TL interface bypass options
- Fully validated

Protocol Compatibility

Standards	Data Rates (Gbps)
PCIe 4.0	16, 8, 5, 2.5

Deliverables

- Core (source code)
- Testbench (source code)
- Complete documentation
- Expert technical support
- Maintenance updates

Overview

The Northwest Logic Expresso 4.0 core from Rambus is designed for maximum performance and ease of use for PCIe 4.0 applications. It is backwards compatible with PCIe 3.0/2.1/1.1 specifications.

The Expresso 4.0 core separately, or in combination with the Northwest Logic family of DMA cores and DMA drivers, provides the maximum system throughput on a PCIe link.

The core is specifically designed for ease of use including full receive packet decoding, complete error handling, automatic handling of PCIe message packets and comprehensive system-debug and link monitoring support.

The core is delivered integrated and verified with the user's target PHY. A complete list of supported PHYs is available on request. To accelerate simulations, the core is also delivered integrated with a fast-simulating behavioral PHY.

The core is provided with the Expresso Testbench which provides a PCIe Bus Functional Model.

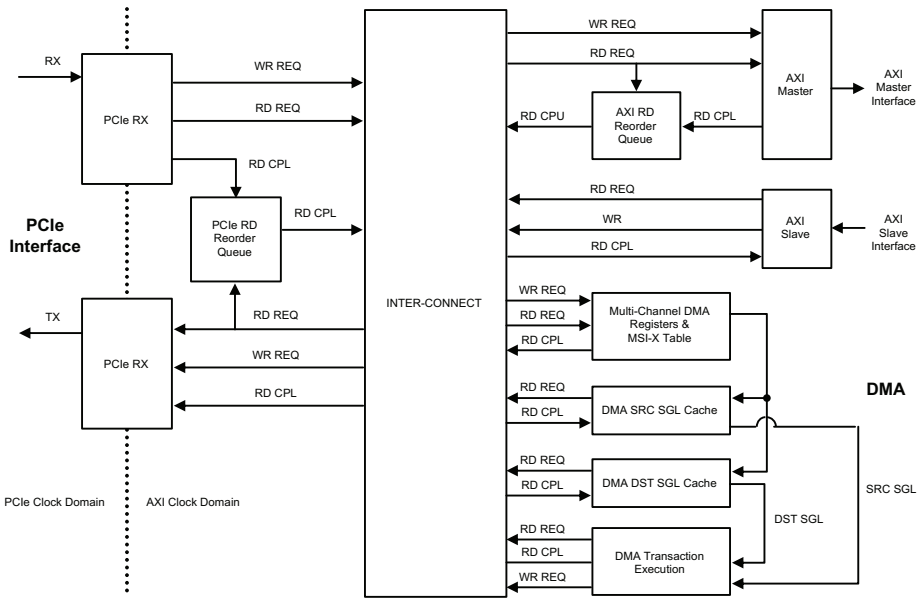
The core is compliant with the current version of the PCIe Base Specification 4.0. The core has been extensively validated with the Avery Design Systems PCI-Xactor PCIe Compliance Suite and Northwest Logic Expresso Testbench.

IP core customization services are also available.

Expresso DMA Bridge Core

The Northwest Logic Expresso DMA Bridge core provides high-performance DMA and/or bridging between PCI Express (PCIe) and AXI for both Endpoint and Root Port applications.

Expresso DMA Bridge Core Block Diagram



Highlights

- Provides high-performance PCIe-AXI Bridge and/or scatter-gather DMA
- Works with Northwest Logic Expresso cores and FPGA PCIe hard cores
- Supports memory-mapped and streaming (FIFO) DMA operation
- Support for up to 1024 DMA Channels
- Supports Endpoint and Root Port applications
- Supports AXI 32, 64, 128 or 256-bit data widths
- Supports PCIe Multi-Function and SRIOV capability
- Fully validated
- Windows and Linux Expresso DMA drivers available

Deliverables

- Core (source code)
- Testbench (source code)
- Complete documentation
- Expert technical support
- Maintenance updates

Overview

The Northwest Logic Expresso DMA Bridge core from Rambus provides high-performance DMA and/or bridging between PCI Express and AXI for both Endpoint and Root Port applications.

The core provides high-performance PCIe-AXI bridge and/or scatter-gather DMA operation. It works with Northwest Logic Expresso cores and FPGA hard cores. It provides complete Root Port Bridging support, and supports memory-mapped/streaming (FIFO) DMA operation. It can be configured with multiple DMA channels which are independently controlled by software. The core provides address translations and security support. It supports legacy, MSI, MSI-X and local AXI interrupts.

Using the core eliminates the need for the user to implement their own DMA and/or bridging design thus significantly reducing the development time and risk.

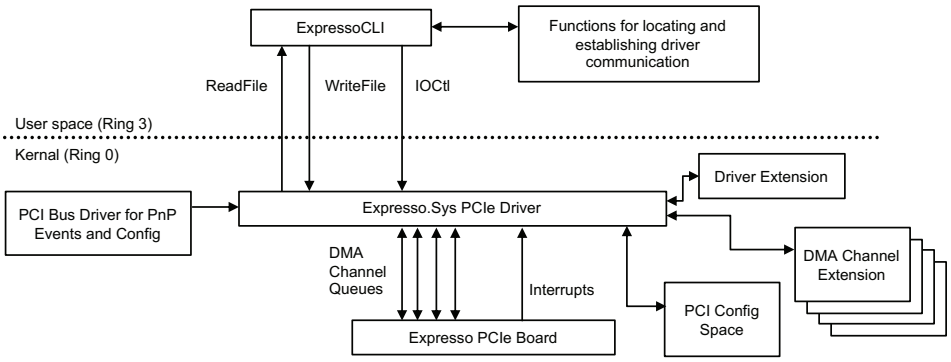
Companion Windows and Linux Expresso DMA drivers are available. The Expresso DMA Driver works hand-in-hand with the Expresso DMA Bridge core.

IP core customization services are also available.

Expresso DMA Driver

The Northwest Logic Expresso DMA Driver is specifically designed to be used with the Expresso DMA Bridge core. It supports all DMA modes supported by the Expresso DMA Bridge core. Together they provide a complete, pre-packaged, flexible DMA solution.

Expresso DMA Driver Environment



Highlights

- Works with Northwest Logic Expresso DMA Bridge core to provide high-performance, scatter-gather DMA operation
- Fully supports overlapped DMA operation
- Supports up to 1024 DMA channels
- Windows and Linux versions share common API
- Supports 32 and 64-bit system addressing
- Supports legacy, MSI, MSI-X and local AXI interrupts
- Performs parameter checking
- Quickly customized to create an application-specific driver
- Includes Command Line Interface (CLI) test application

Deliverables

- Driver source code (C)
- Developer's guide
- Expert technical support
- Maintenance updates

Overview

The Northwest Logic Expresso DMA Driver from Rambus is specifically designed to be used with the Expresso DMA Bridge core. It supports all DMA modes supported by the Expresso DMA Bridge core. Together the driver and core provide a complete, pre-packaged, flexible DMA system.

The Expresso DMA Driver includes support for device registers and memory reads and writes, DMA read-and-write transfers, low-level performance statistics, PnP and Power Management events (Windows), and legacy, MSI and MSI-X interrupts.

The driver creates and manages descriptor chains in system memory. It then fetches and executes these descriptor chains. This approach enables the descriptor chain size to be maximized while minimizing the need for large descriptor memories in the Expresso DMA Bridge core.

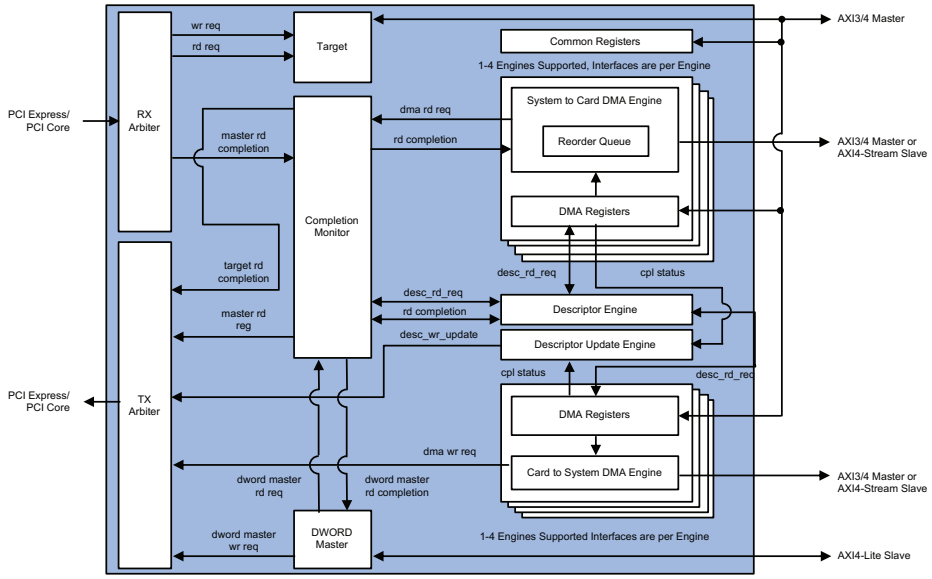
Windows and Linux versions of the Expresso DMA driver have been designed for maximum API compatibility to facilitate application porting between Windows and Linux. A CLI test application is provided which can read and write large quantities of data, collect performance data, etc.

IP core customization services are also available.

AXI DMA Back-End Core

The Northwest Logic AXI DMA Back-End core provides high-performance, scatter-gather DMA operation in a flexible fashion. It can be easily integrated and used in a wide variety of DMA-based systems.

AXI DMA Back-End Core Block Diagram



Highlights

- Provides high-performance scatter-gather DMA operation
- Works with Northwest Logic Expresso cores and FPGA PCIe hard cores
- Can be configured with multiple independent DMA engines
- Supports Packet/Block and Addressed/Non-addressed transfers
- AXI3/4 and AXI4-Stream interfaces
- Supports 32 and 64-bit system addressing
- Supports legacy, MSI, MSI-X interrupts
- Fully hardware validated
- Windows and Linux
- DMA drivers available
- Provided with PCI Express Testbench
- Delivered fully integrated with target PCIe PHY

Deliverables

- Core (source code)
- Testbench (source code)
- Complete documentation
- Expert technical support
- Maintenance updates

Overview

The Northwest Logic AXI DMA Back-End core from Rambus provides high-performance, scatter-gather DMA operation in a flexible fashion. The core can be easily integrated and used in a wide variety of DMA-based systems.

The core works with Northwest Logic Expresso cores and FPGA hard cores. It can be configured with multiple DMA Engines which each have their own interface. It supports Packet/Block and Addressed/Non-addressed transfers. Host-based and local descriptors are supported. The core supports legacy, MSI and MSI-X interrupts.

Using the core eliminates the need for the user to implement their own DMA design thus significantly reducing the development time and risk.

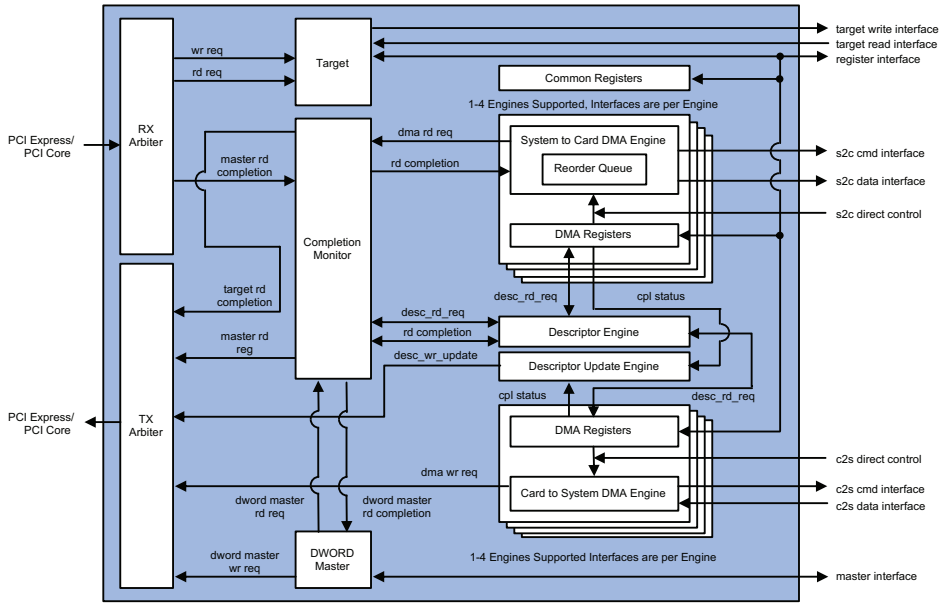
Companion Windows and Linux DMA drivers are available. The DMA Back-End Driver works hand-in-hand with the AXI DMA Back-End core to implement host-based, scatter-gather DMA operation.

IP core customization services are also available.

DMA Back-End Core

The Northwest Logic DMA Back-End core provides high-performance, scatter-gather DMA operation in a flexible fashion. It can be easily integrated and used in a wide variety of DMA-based systems.

DMA Back-End Core Block Diagram



Highlights

- Provides high-performance scatter-gather DMA operation
- Works with Northwest Logic Expresso cores and FPGA PCIe hard cores
- Can be configured with multiple independent DMA engines
- Supports Packet/Block and Addressed/Non-addressed transfers
- Supports 32 and 64-bit system addressing
- Supports legacy, MSI, MSI-X interrupts
- Fully hardware validated
- Windows and Linux DMA drivers available
- Provided with PCI Express Testbench
- Delivered fully integrated with target PCIe PHY

Deliverables

- Core (source code)
- Testbench (source code)
- Complete documentation
- Expert technical support
- Maintenance updates

Overview

The Northwest Logic DMA Back-End core from Rambus provides high-performance, scatter-gather DMA operation in a flexible fashion. The core can be easily integrated and used in a wide variety of DMA-based systems.

The core works with Northwest Logic Expresso cores and FPGA hard cores. It can be configured with multiple DMA Engines which each have their own interface. It supports Packet/Block and Addressed/Non-addressed transfers. Host-based and local descriptors are supported. The core supports legacy, MSI and MSI-X interrupts.

Using the core eliminates the need for the user to implement their own DMA design thus significantly reducing the development time and risk.

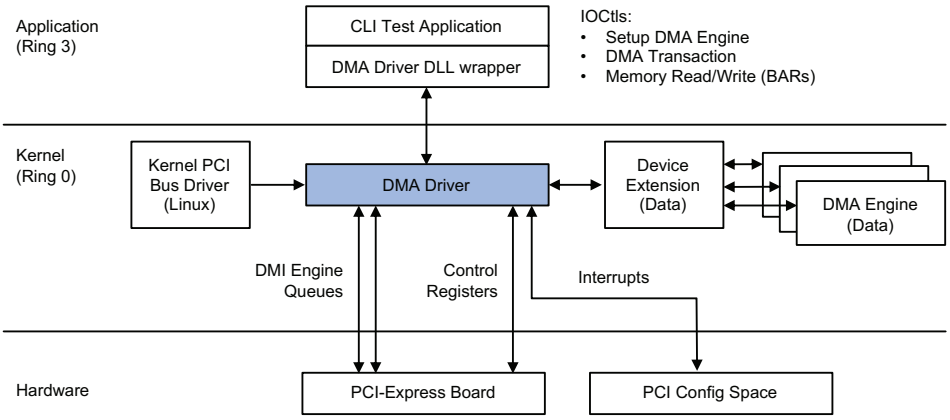
Companion Windows and Linux DMA drivers are available. The DMA Back-End Driver works hand-in-hand with the DMA Back-End core to implement host-based, scatter-gather DMA operation.

IP core customization services are also available.

DMA Back-End Driver

The Northwest Logic DMA Back-End Driver is designed to be used with the Northwest Logic AXI DMA Back-End core. It supports all DMA modes supported by the core including Packet/Block and Addressed/Non-Addressed transfers.

DMA Back-End Driver Environment



Overview

The Northwest Logic DMA Back-End Driver from Rambus is designed to be used with the Northwest Logic DMA Back-End core and AXI DMA Back-End core. It supports all DMA modes supported by the core including Packet/Block and Addressed/Non-Addressed transfers. Together the driver and core provide a complete, pre-packaged, flexible DMA system.

The DMA Back-End Driver includes support for a) device registers and memory reads and writes, b) DMA read and write transfers, c) low-level performance statistics, d) PnP and Power Management events (Windows), and e) legacy, MSI and MSI-X interrupts.

The DMA Back-End Driver creates and manages descriptor chains in system memory. The DMA core then fetches and executes these descriptor chains. This approach enables the descriptor chain size to be maximized while minimizing the need for large descriptor memories in the DMA core.

Companion Windows and Linux Expresso DMA drivers are available. API compatibility simplifies application porting.

IP core customization services are also available.

Highlights

- Works with Northwest Logic AXI DMA Back-End core to provide high-performance, scatter-gather DMA operation
- Fully supports overlapped DMA operation
- Windows and Linux versions use common API
- Supports Packet/Block and Addressed/Non-addressed transfers
- Supports 32 and 64-bit system addressing
- Supports legacy, MSI, MSI-X interrupts
- Performs parameter checking
- Can be quickly customized to create an application-specific driver
- Includes Command Line Interface (CLI) test application

Deliverables

- Driver source code (C)
- Developer's guide
- Expert technical support
- Maintenance updates

Rambus

PCI Express Solution – FAQ

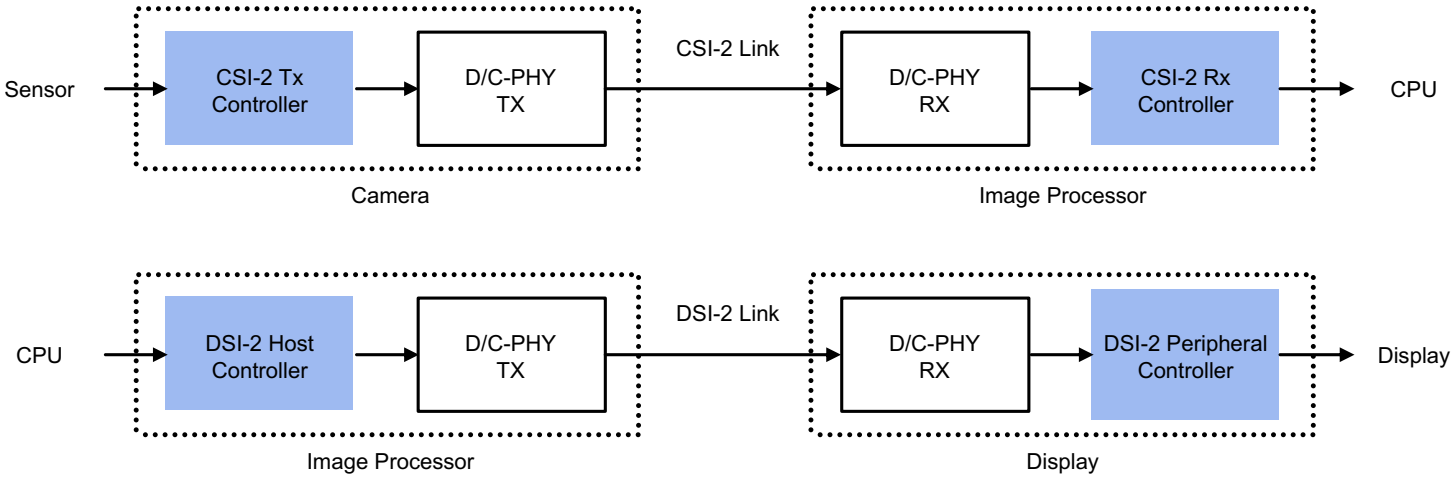
1. **What differentiates Rambus PCI Express Solution from other vendor's cores?**
   - Complete solution- Rambus provides a complete solution for PCI Express including Cores, Drivers, Demonstration Applications and Development Board binaries minimizing customer development time, cost and risk.
   - Ease-of-Use- The DMA Core provides a pre-packaged back-end design which can be used with Rambus Expresso (PCIe) soft Core or with FPGA hard PCIe Cores.
   - High-Throughput- The cores are specifically designed to enable high-throughput designs including support for larger pay-loads, DMA transactions, etc.
   - Usable in both FPGAs and ASICs- Allows a design to be prototyped in an FPGA before creating the ASIC.
   - Comprehensive PCI Express PHY support including PIPE-compliant ASIC PHYs, FPGAs integrated PHY and discrete PHY chips
   - Testbench – Each core is provided with a Testbench containing a PCI Express bus functional model with traffic generation and capture capabilities.
   - Source code available
   - Expert Support- Fast turnaround support is provided by the actual designers.
   - Customization & Integration Services- Rambus is available to customize the cores to meet your unique needs and integrate the cores with additional logic.

2. **Can I use the Expresso Solution in an ASIC?**
   - Rambus delivers the solution pre-configured for use in an ASIC. This includes integration and verification with the target PCI Express PHY.
   - Rambus supports a broad range of PCI Express PHYs. Contact Rambus for more information.
   - Rambus PCI Express Solution has been used in a variety of different ASIC designs. Contact Rambus for more information.

3. **Can I use the Expresso Solution in an FPGA?**
   - Rambus supports all of the internal PHY FPGAs and all of the external PHY chips.
   - Rambus PCI Express Solution Cores were specifically designed to achieve the maximum possible performance in an FPGA with a minimum number of constraints. This was achieved by minimizing the amount of logic and careful use of pipelining.
   - Rambus PCIe Cores all support a wide variety of FPGA-based boards which can be used to prototype a design including Rambus PCI Express Solution. Contact Rambus for more information.

Rambus

MIPI Solution Overview



Solution Includes:

- **CSI-2 Controller Cores**
  - Fully CSI-2 standard compliant
  - 1-8, 2.5+ Gbit/s D-PHY data lane support
  - 1-4, 2.5+ Gsym/s C-PHY lane (trio) support
  - Support Low Power, High Speed modes
  - Support for all data types
  - Easy to use pixel-based user interface
  - Optional Video Interface
- **DSI-2 Controller Cores**
  - Fully DSI-2/DSI standard compliant
  - 1-4, 2.5+ Gbit/s D-PHY data lane support
  - 1-4, 2.5+ Gsym/s C-PHY lane (trio) support
  - Supports Low Power including Reverse Data and High Speed modes
  - Support for all data types
  - Easy to use packet-based user interface
  - Optional DSI-2 Video interface

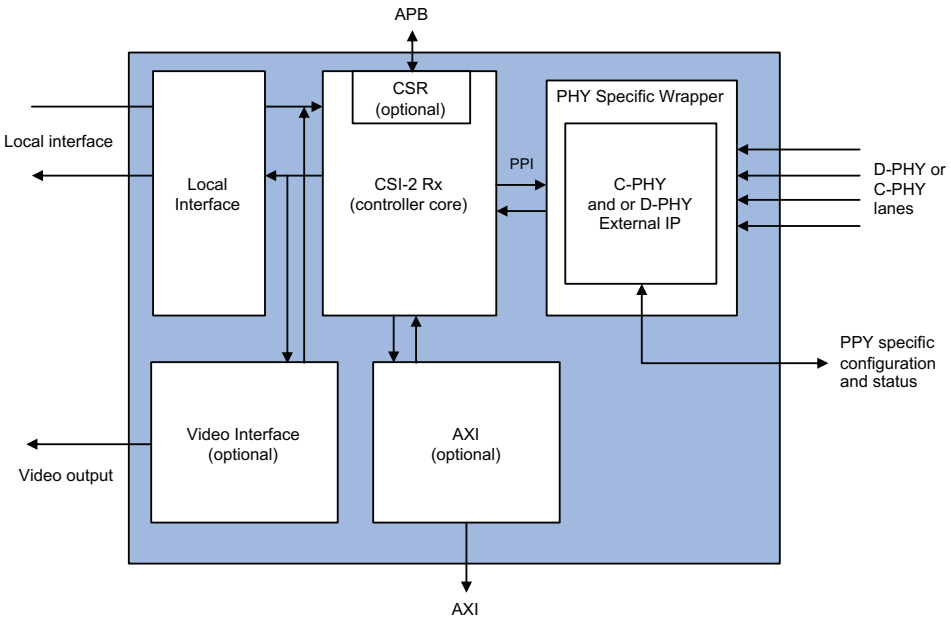
Key Features:

- **Complete Solution**
  - Supports all CSI-2, DSI-2/DSI flavors
  - Transmit (Host) and Receive (Peripheral)
  - Provided with MIPI Testbench
  - Flexible PHY interface supports 8/16/32 bit/lane PPI compatible PHYs
  - Delivered fully integrated and verified with target MIPI PHY
  - Power consumption minimized via clock gating
  - Minimal ASIC gate count
  - Silicon proven
- **High Performance**
  - Supports maximum data rates specified by the CSI-2, DSI-2/DSI standards
  - Minimal latency
- **Easy-To-Use**
  - Simple interface, easy to configure, well-documented
- **Comprehensive Support**
  - ASIC, Structured ASIC and FPGA support
  - Expert technical support provided directly by designers
  - Integration and customization services available

CSI-2 Controller Core V2

The Northwest Logic CSI-2 controller core is a second-generation CSI-2 core optimized for high performance, low power and small size.

CSI-2 Controller V2 Block Diagram (Receive Version)



Highlights

- Fully CSI-2 standard compliant
- 64 and 32-bit core widths
- Transmit and Receive versions
- 1-8, 2.5+ Gbps D-PHY data lanes
- 1-4, 2.5+ Gsym/s C-PHY lane (trio)
- Optional video interface
- Easy-to-use pixel-based interface
- Delivered fully integrated and verified with target MIPI PHY
- Provided with CSI-2 testbench

Protocol Compatibility

Standards	Data Rate
CSI-2	2.5+ Gbps/lane

Deliverables

- Core (source code)
- Testbench (source code)
- Complete documentation
- Expert technical support
- Maintenance updates

Overview

The Northwest Logic CSI-2 Controller Core V2 from Rambus is optimized for high performance, low power and small size.

It is available in 64 and 32-bit core widths. The 64-bit core width supports 1-8 D-PHY data lanes (8-bit PPI) and 1-4 C-PHY lanes (16-bit PPI). The 32-bit core width supports 1-4 D-PHY data lanes (8-bit PPI) and 1-2 C-PHY lanes (16-bit PPI).

The core is fully compliant with the CSI-2 standard and implements all three layers defined therein: Pixel to Byte Packing, Low Level Protocol, and Lane Management. Separate Transmit (Tx) and Receive (Rx) versions of the core are available.

The core's local interface provides an easy-to-use pixel based interface (single, double, quad, octal pixel wide). An optional AXI interface is available for the CSI-2 Rx Controller Core. An optional Hsync/Vsync video interface is also available.

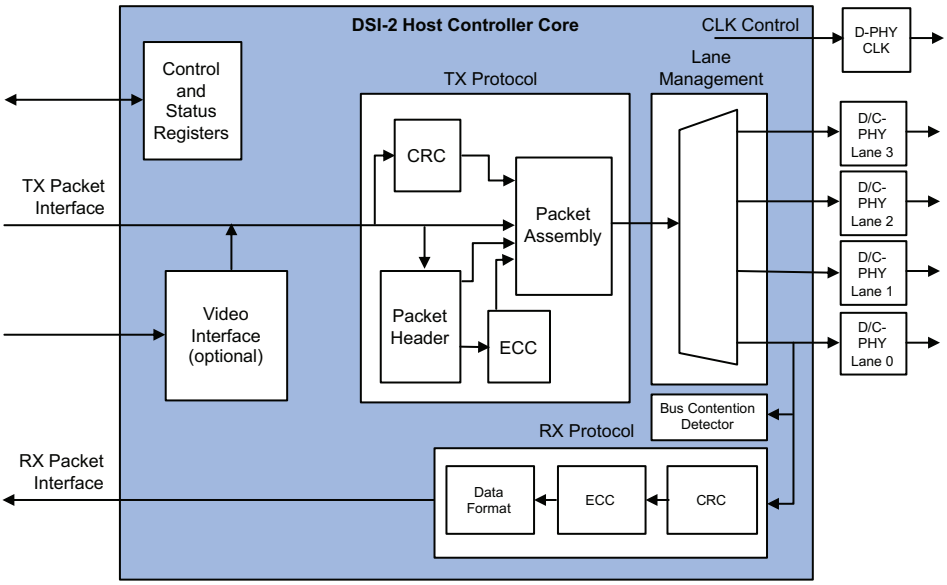
The core is delivered fully integrated and verified with the user's target D/C-PHY. Please contact Rambus for a complete list of supported PHYs.

The core is also provided with the CSI-2 Testbench which provides a CSI-2 Bus Functional Model.

DSI-2 Controller Core

The Northwest Logic DSI-2 controller core is a second-generation DSI core optimized for high performance, low power and small size.

DSI-2 Controller Block Diagram (Host Version)



Highlights

- Fully DSI-2/DSI standard compliant
- 64 and 32-bit core widths
- Host (Tx) and Peripheral (Rx) versions
- 1-4, 2.5+ Gbps D-PHY data lanes
- 1-4, 2.5+ Gsym/s C-PHY lane (trio)
- Supports all data types
- Easy-to-use native interface
- Delivered fully integrated and verified with target MIPI PHY
- Provided with DSI-2 testbench

Protocol Compatibility

Standards	Data Rate
DSI-2/DSI	2.5+ Gbps/lane

Deliverables

- Core (source code)
- Testbench (source code)
- Complete documentation
- Expert technical support
- Maintenance updates

Overview

The Northwest Logic DSI-2 Controller core from Rambus is optimized for high performance, low power and small size.

It is available in 64 and 32-bit core widths. The 64-bit core width supports 1-4 D-PHY data lanes (8-bit PPI) and 1-4 C-PHY lanes (16-bit PPI). The 32-bit core width supports 1-4 D-PHY data lanes (8-bit PPI) and 1-2 C-PHY lanes (16-bit PPI).

The core is fully compliant with the DSI-2 standard and implements all three layers defined therein: Pixel to Byte Packing, Low Level Protocol, and Lane Management. Separate Host (Tx) and Peripheral (Rx) versions of the core are available.

The core's native interface provides easy-to-use data and control/status packet interfaces. The data interface includes an optional DSI-2 video interface. The interface supports command and video modes and all data types.

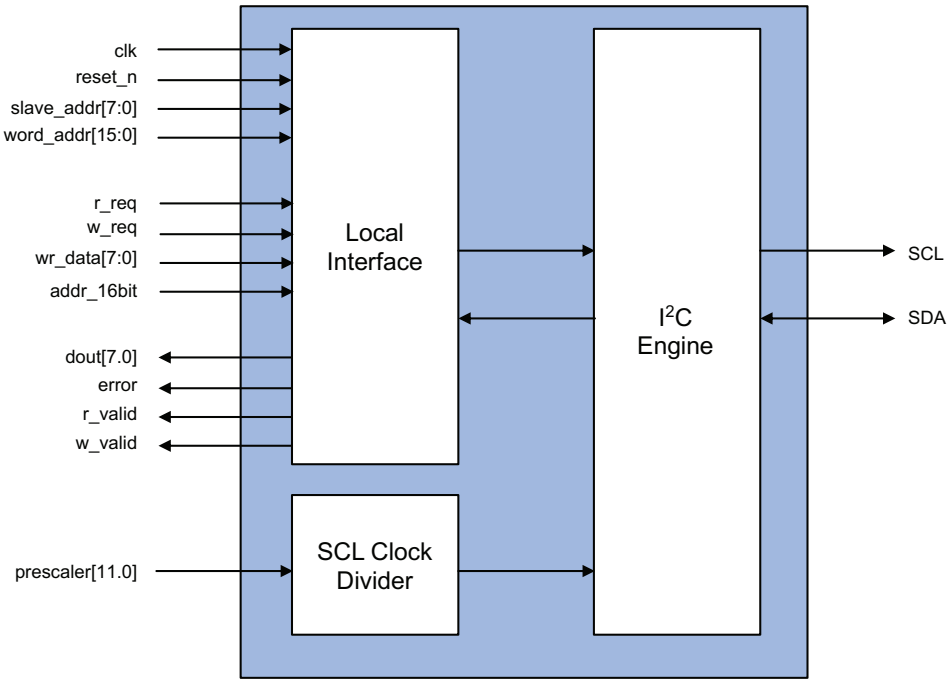
The core is delivered fully integrated and verified with the user's target D/C-PHY. Please contact Rambus for a complete list of supported PHYs.

The core is also provided with the DSI-2 Testbench which provides a DSI-2 Bus Functional Model.

I²C Controller Core

The Northwest Logic I2C Controller Core eliminates the extra logic and complexity of standard I2C controllers to provide a core which is compact, easy to use and customizable.

I²C Controller Block Diagram



Highlights

- Ideal for Serial Presence Detection (SPD) and other I²C applications
- Compact
- Easy to use
- Supports Master/Slave operation
- Simple user interface
- Supports Fast and Standard Modes
- 8 and 16-bit addressing
- Can directly connect to Tx and Rx FIFOs
- Source code available

Deliverables

- Core (source code)
- Testbench (source code)
- Complete documentation
- Expert technical support
- Maintenance updates

Overview

The Northwest Logic I²C Controller core from Rambus eliminates the extra logic and complexity of standard I²C controllers providing a core which is compact, easy to use and customizable.

The core is ideal for performing Serial Presence Detection (SPD) of a memory module and connecting to other I²C devices such as EEPROMs and A/D and D/A converters.

The core supports master and slave operation of an I²C compatible serial bus including Standard and Fast Mode operation. The core also supports 8 and 16-bit addressing.

IP core customization and integration services are available.

Rambus

MIPI Solution – FAQ

1. **What differentiates Rambus MIPI Solution from other vendor's cores?**
   - Complete Solution- Rambus provides a complete solution for MIPI including Cores and MIPI Camera/ Display Demonstration Systems minimizing customer development time, cost and risk.
   - Low Clock Rate- The cores work off of the byte lane clock minimizing power consumption and easing timing closure in older process technologies.
   - Small size – The cores are significantly smaller than other ASIC offerings.
   - Ease-Of-Use – The cores have a very simple interface, require minimal constraints and are uniquely optimized for each device family.
   - Run-time programmability – All parameters are run-time programmable.
   - Usable in both FPGAs and ASICs – Allows a design to be prototyped in an FPGA before creating the ASIC.
   - Source code available
   - Comprehensive MIPI PHY support
   - Testbench – Each core is provided with a Testbench containing a MIPI bus functional model with traffic generation and capture capabilities.
   - Expert Support – Fast turnaround support is provided by the actual designers.
   - Customization & Integration Services – Rambus is available to customize the cores to meet your unique needs and integrate the cores with additional logic.

2. **Can I use the MIPI Solution in an ASIC?**
   - Rambus delivers the solution pre-configured for use in an ASIC. This includes integration and verification with the target MIPI PHY.
   - Rambus supports a broad range of MIPI PHYs. Contact Rambus for more information.
   - Rambus MIPI Solution has been used in a variety of different ASIC designs. Contact Rambus for more information.

3. **Can I use the MIPI Solution in an FPGA?**
   - Rambus MIPI Solution Cores were specifically designed to achieve the maximum possible performance in an FPGA with a minimum number of constraints. This was achieved by minimizing the amount of logic and careful use of pipelining.
   - Rambus has created CSI-2 Camera and DSI Display FPGA-based demonstration systems. Contact Rambus for more information.

For more information, visit
rambus.com/interface-ip/controllers/